S5KJNSSQ33

1/2.76" 50Mp for 12.5Mp Tetra CMOS Image Sensor

Revision 0.05

Jun 2022

Data Sheet

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Chip Handling Guide

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2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
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0.01	Jun 02, 2022	• Updated Table 26	Ritesh Solanki
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0.05	Jun 17, 2022	• Part ID has been updated (SQ23 → SQ33)	Heegeun Park

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Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
RW	Read/Write	The application has permission to read and writes in the Register field. Written value effects on the next frame.
RW/R	Read/Write	The application has permission to read and writes in the Register field. Written value effects only on exit from stand-by.
RW/C	Read/Write	The application has permission to read and writes in the Register field. Changing value typically causes configuration change (either in abort timing or preserve timing modes).
RW/SR	Read/Write	The application has permission to read and writes in the Register field. Changing value may cause entering stand-by / software reset.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

1 Product Overview

1.1 Introduction

S5KJNSSQ33 is a highly integrated 50MP for 12.5 MP Tetra Bayer (also referred as TetraCell) which is summation of every 4 pixels with same color into one big pixel. This camera chip includes a CMOS Image Sensor (CIS), image correction functionality and serial transmission capability using 4-lane MIPI. It is designed for fast and low-power operation to deliver full resolution capture at 30 frames per second (fps) and 4K video at 60 fps.

S5KJNSSQ33 has 2x2 Tetra-Cell RGB Bayer pattern. Each color channel of 2x2 Tetra-Cell RGB Bayer pattern is composed of four pixels of one color filter and its shape is 2x2 square. S5KJNSSQ33 supports binning output mode only in which the adjacent same color pixels are summed.

S5KJNSSQ33 is fabricated by the Samsung CMOS image sensor process, which realizes a high-efficiency and low-power photo sensor. The sensor consists of 8160x6144 physical pixels (4080x3072 effective pixels) that meets the 1/2.76-inch optical format.

S5KJNSSQ33 CIS has on-chip 10-bit ADC arrays to digitize the pixel output and on-chip Correlated Double Sampling (CDS) to drastically reduce Fixed Pattern Noise (FPN). It incorporates on-chip camera functions such as dark level compensation, defect correction, exposure setting, and white balance setting.

S5KJNSSQ33 CIS is programmable through a CCI or SPI serial interface and includes on-chip One-Time Programmable (OTP) Non-Volatile Memory (NVM).

S5KJNSSQ33 is suitable for a low-power camera module with a 2.8 V/1.8 V/1.05 V power supply.

1.2 Features

S5KJNSSQ33 supports the following features:

- 50MP for 12.5 MP Tetra sensor with 1/2.76-inch optics
- Unit pixel size: 0.64 μm (Effectively 1.28μm)
- Physical resolution: 8160 (H) × 6144 (V)
- Effective resolution: 4080 (H) × 3072 (V)
- Active resolution: 4096 (H) × 3088 (V)
- Color filter: RGB Bayer pattern
- Shutter type: Electronic rolling shutter and global reset
- Max. normal frame rate: 30 fps @ Full
- Max. video frame rate: 60fps @ 4K
- Data rate: 2,150 Mbps/lane
- ADC accuracy: 10 bits
- Super PD for faster autofocus even in dark environments
- Dual sensor synchronize
- Interfaces
  - Fine interface frequency control using additional dedicated PLL for integration flexibility and to avoid EMI
  - MIPI CSI2: 4 lanes (2.15 Gbps per lane)
  - Output formats: RAW10
- Control interface
  - SPI interface: Four-wire serial communication circuit up to 20 MHz
  - Camera Control Interface (CCI) high-speed I2C-compatible - Two-wire serial communication circuit up to 1 MHz
- 512Bytes of On-chip OTP memory for users
- Maximum Analog Gain of x64 : Full mode
- Vertical flip and horizontal mirror mode
- Mapped bad pixel correction
- Interscene DCG function
- Built-in test pattern generation
- Supply voltage: 2.8 V for analog, 1.8 V for I/O, and 1.05 V for digital core supply
- Operating temperature: -20℃ to +85℃

2 Pad Configuration

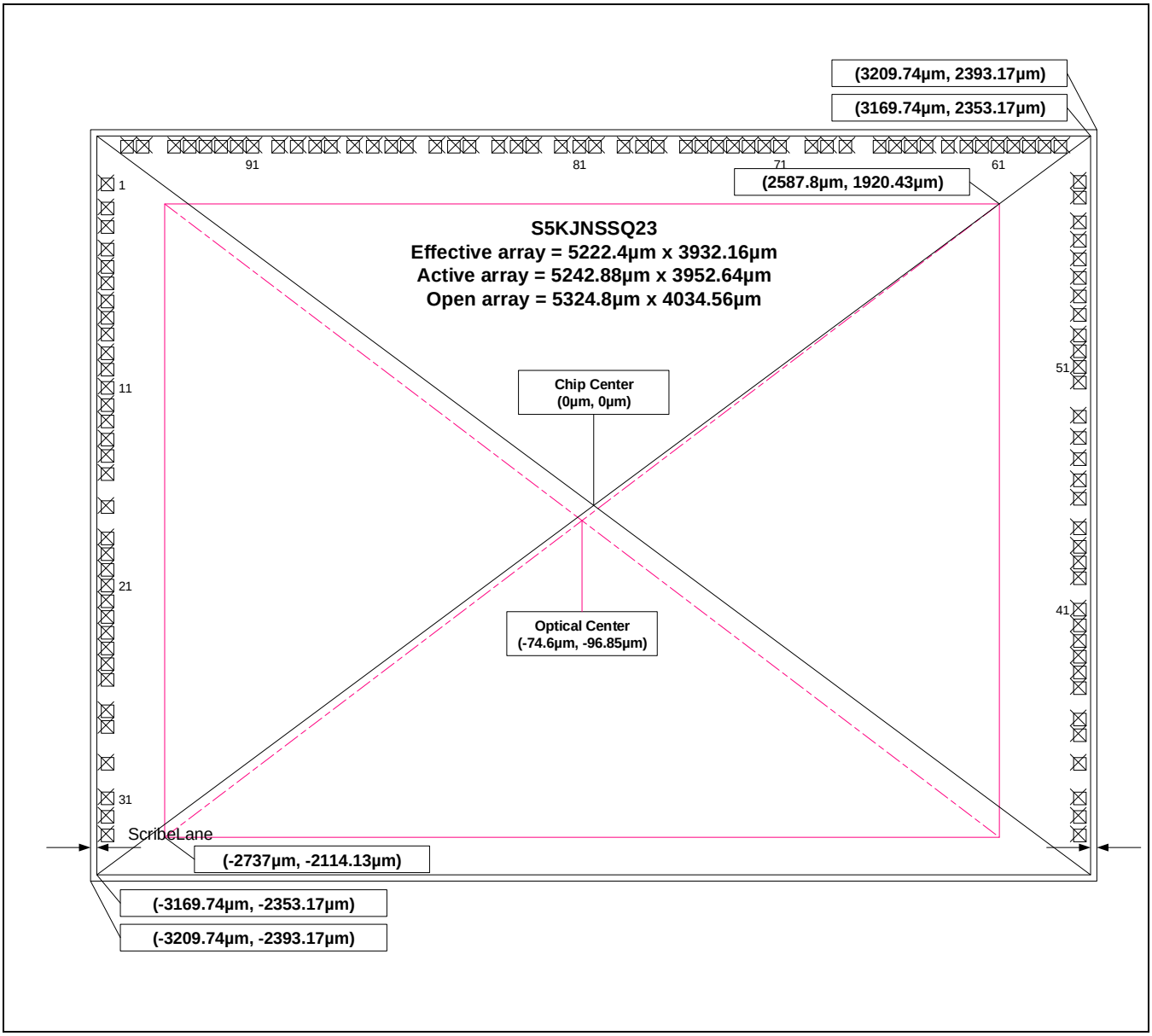

Figure 1 Chip Dimension Top View

2.1 Pad Description

- Origin = Center of chip
- NC = Not Connected, P = POWER, G = GROUND, S = SIGNAL

Table 1 Pad Description

Pad No.	Pad Name	Type	A/D	X-Axis	Y-Axis	Description
1	VDDD_MIPI	P	D	-3101.44	2044.36	MIPI 1.05V Digital Power
2	VDDA_MIPI	P	A	-3101.44	1891.23	2.8V MIPI Power
2-1	Dummy			-3101.44	1773.23	Not Connected
3	VSSD_MIPI	G	D	-3101.44	1629.36	MIPI Digital Ground
4	M_DNDATA0	S	A	-3101.44	1518.73	DPHY Data Negative 0
5	M_DPDATA0	S	A	-3101.44	1414.66	DPHY Data Positive 0
6	M_DNDATA1	S	A	-3101.44	1298.73	DPHY Data Negative 1
7	M_DPDATA1	S	A	-3101.44	1194.66	DPHY Data Positive 1
8	VSSD	G	D	-3101.44	1088.73	Digital Ground
9	M_DNCLK	S	A	-3101.44	968.73	DPHY Clock Negative
10	M_DPCLK	S	A	-3101.44	864.66	DPHY Clock Positive
11	VDDD	P	D	-3101.44	748.73	1.05V Digital Power
12	M_DNDATA2	S	A	-3101.44	638.73	DPHY Data Negative 2
13	M_DPDATA2	S	A	-3101.44	534.66	DPHY Data Positive 2
14	M_DNDATA3	S	A	-3101.44	418.73	DPHY Data Negative 3
15	M_DPDATA3	S	A	-3101.44	314.66	DPHY Data Positive 3
16	VSSD_MIPI	G	D	-3101.44	199.36	MIPI Digital Ground
17	VDDD_MIPI	P	D	-3101.44	-10.64	MIPI 1.05V Digital Power
18	VDDD	P	D	-3101.44	-210.64	1.05V Digital Power
19	VSSD	G	D	-3101.44	-310.64	Digital Ground
20	GPIO_1	S	D	-3101.44	-410.64	General I/O 1

21	VSYNC	S	D	-3101.44	-510.64	VSYNC Signal
22	GPIO_3	S	D	-3101.44	-610.64	General I/O 3
23	VDDIO	P	D	-3101.44	-710.64	IO Power
24	VDDD	P	D	-3101.44	-811.34	1.05V Digital Power
25	VDDD	P	D	-3101.44	-911.34	1.05V Digital Power
26	VSSD	G	D	-3101.44	-1011.34	Digital Ground
27	VSSD	G	D	-3101.44	-1111.34	Digital Ground
28	VSSA	G	A	-3101.44	-1311.34	Analog Ground
29	VDDA	P	A	-3101.44	-1411.34	2.8V Analog Power
30	Dummy			-3101.44	-1645.81	Not Connected
31	VSSA	G	A	-3101.44	-1865.98	Analog Ground
31-1	Dummy			-3101.44	-1983.98	Not Connected
31-2	Dummy			-3101.44	-2101.98	Not Connected
31-3	Dummy			3101.44	-2102.61	Not Connected
31-4	Dummy			3101.44	-1984.61	Not Connected
32	VSSA	G	A	3101.44	-1866.61	Analog Ground
33	Dummy			3101.44	-1646.44	Not Connected
34	VDDA	P	A	3101.44	-1463.97	2.8V Analog Power
35	VSSA	G	A	3101.44	-1363.97	Analog Ground
36	VSSD	G	D	3101.44	-1163.97	Digital Ground
37	VSSD	G	D	3101.44	-1063.97	Digital Ground
38	VDDD	P	D	3101.44	-963.97	1.05V Digital Power
39	VDDD	P	D	3101.44	-863.97	1.05V Digital Power
40	VSSA	G	A	3101.44	-763.97	Analog Ground
41	VDDA	P	A	3101.44	-663.97	2.8V Analog Power

42	Dummy			3101.44	-463.97	Not Connected
43	VSSA	G	A	3101.44	-363.97	Analog Ground
44	VDDA	P	A	3101.44	-263.97	2.8V Analog Power
44-1	Dummy			3101.44	-145.97	Not Connected
45	VNTG	S	A	3101.44	42.03	Connect to Cap. C3
46	VTG	S	A	3101.44	159.53	Connect to Cap. C4
47	VSEL	S	A	3101.44	294.53	Connect to Cap. C5
48	VRG2	S	A	3101.44	429.53	Connect to Cap. C6
49	VRG1	S	A	3101.44	564.53	Connect to Cap. C7
50	Dummy			3101.44	782.03	Not Connected
51	VDDA	P	A	3101.44	882.03	2.8V Analog Power
52	VSSA	G	A	3101.44	982.03	Analog Ground
53	VDDD	P	D	3101.44	1082.03	1.05V Digital Power
54	VSSD	G	D	3101.44	1213.03	Digital Ground
54-1	Dummy			3101.44	1331.03	Not Connected
54-2	Dummy			3101.44	1449.03	Not Connected
54-3	Dummy			3101.44	1567.03	Not Connected
54-4	Dummy			3101.44	1685.03	Not Connected
54-5	Dummy			3101.44	1803.03	Not Connected
55	VSSA	G	A	3101.44	1960.47	Analog Ground
56	VDDA	P	A	3101.44	2060.47	2.8V Analog Power
57	HSYNC	S	D	2977.04	2284.87	Horizontal Sync signal
58	VSYNC_IN	S	D	2877.04	2284.87	Vertical sync input to enable dual sensor function
59	Dummy			2777.04	2284.87	Not Connected

60	Dummy			2677.04	2284.87	Not Connected
61	Dummy			2577.04	2284.87	Not Connected
62	VDDIO	P	D	2477.04	2284.87	IO Power
63	GPIO_2	S	D	2377.04	2284.87	General I/O 2
63-1	Dummy			2259.04	2284.87	Not Connected
64	VDDD	P	D	2123.04	2284.87	1.05V Digital Power
65	VSSD	G	D	2023.04	2284.87	Digital Ground
66	I2C_SPI_N_SEL	S	D	1923.04	2284.87	SPI/CCI Select (1: CCI, 0: SPI)
67	I2C_ID1	S	D	1823.04	2284.87	MSB bit of CCI Slave Address Selection
68	Dummy			1605.54	2284.87	Not Connected
69	VSSA	G	A	1488.04	2284.87	Analog Ground
70	VDDA	P	A	1388.04	2284.87	2.8V Analog Power
71	XCE	S	D	1188.04	2284.87	LSB bit of CCI Slave Address Selection
72	SDO	S	D	1088.04	2284.87	SPI mode: Serial Data output / CCI mode: leave open
73	VDDIO	P	D	988.04	2284.87	IO Power
74	SCK	S	D	888.04	2284.87	CCI Clock, connect external 2.2KOhm resistor
75	SDI	S	D	788.04	2284.87	CCI Data, connect external 2.2KOhm resistor
76	Dummy			688.04	2284.87	Not Connected
77	Dummy			588.04	2284.87	Not Connected
78	VDDD	P	D	407.96	2284.87	1.05V Digital Power
79	VSSD	G	D	307.96	2284.87	Digital Ground
79-1	Dummy			189.96	2284.87	Not Connected
80	VDDD	P	D	7.96	2284.87	1.05V Digital Power

81	VSSD	G	D	-92.04	2284.87	Digital Ground
81-1	Dummy			-210.04	2284.87	Not Connected
82	VDDD	P	D	-392.04	2284.87	1.05V Digital Power
83	VSSD	G	D	-492.04	2284.87	Digital Ground
83-1	Dummy			-610.04	2284.87	Not Connected
84	VDDD	P	D	-792.04	2284.87	1.05V Digital Power
85	VSSD	G	D	-892.04	2284.87	Digital Ground
85-1	Dummy			-1010.04	2284.87	Not Connected
86	VDDD	P	D	-1192.04	2284.87	1.05V Digital Power
87	VSSD	G	D	-1292.04	2284.87	Digital Ground
87-1	Dummy			-1410.04	2284.87	Not Connected
88	VDDA_PLL	P	A	-1534.54	2284.87	2.8V PLL Power
89	VSS_PLL	G	D	-1677.04	2284.87	PLL Digital Ground
90	VDDD_PLL	P	D	-1777.04	2284.87	1.05V PLL Power
90-1	Dummy			-1895.04	2284.87	Not Connected
90-2	Dummy			-2013.04	2284.87	Not Connected
91	VDDIO	P	D	-2177.04	2284.87	IO Power
92	VDDD	P	D	-2277.04	2284.87	1.05V Digital Power
93	VSSD	G	D	-2377.04	2284.87	Digital Ground
94	MCLK	S	D	-2477.04	2284.87	External Input Clock
95	RSTN	S	D	-2577.04	2284.87	Master Reset, active low
96	TST	S	D	-2677.04	2284.87	Digital Ground
97	VSSA	G	A	-2877.04	2284.87	Analog Ground
98	VDDA	P	A	-2977.04	2284.87	2.8V Analog Power

2.2 Application Circuit

Figure 2 illustrates the top view of a module application circuit.

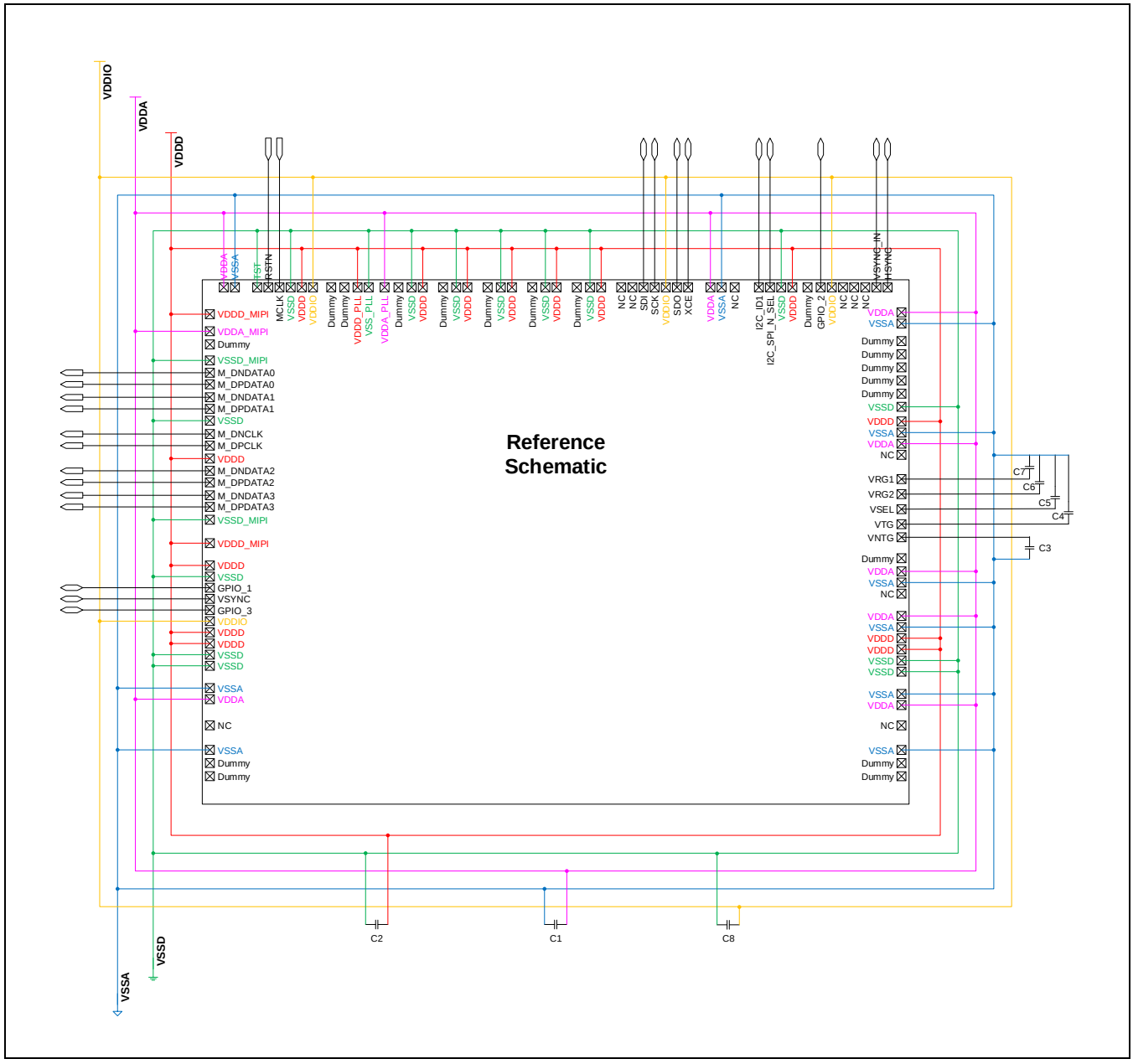

Figure 2 Top View of Module Application Circuit

2.3 Pixel Array Information

Figure 3 illustrates the top view of pixel array information.

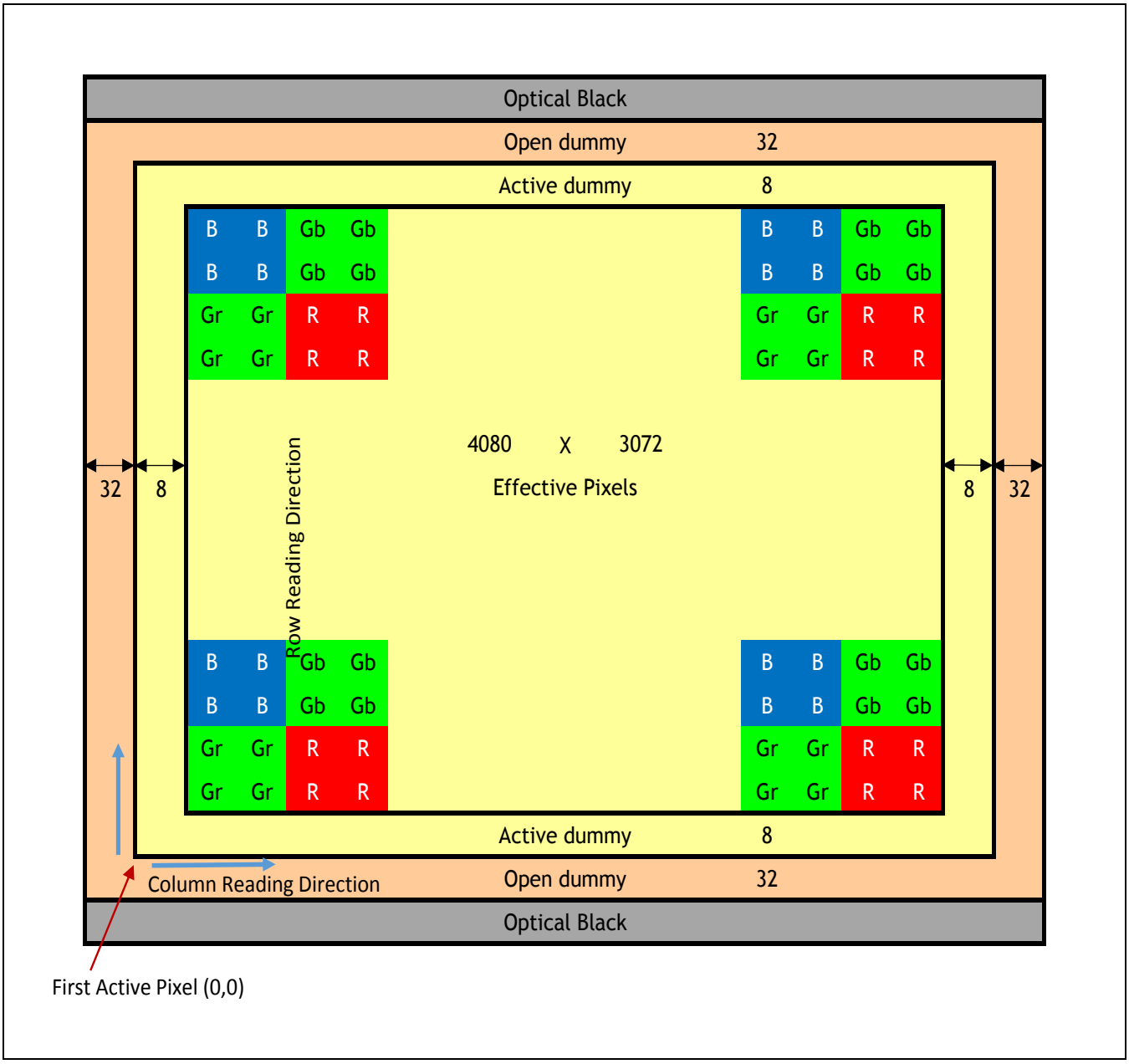

Figure 3 Top View of Pixel Array Information

3 Power Sequence

3.1 Operating Modes

Table 2 describes sensor module has four operating modes. Moving from one mode to another is achieved by issuing the appropriate mode command through CCI serial control interface, RSTN (XSHUTDOWN) signal changing states and power supplies. S5KJNSSQ33 powers up with CSI-2 serial data interface enabled. Figure 4 illustrates valid mode changes for the sensor module.

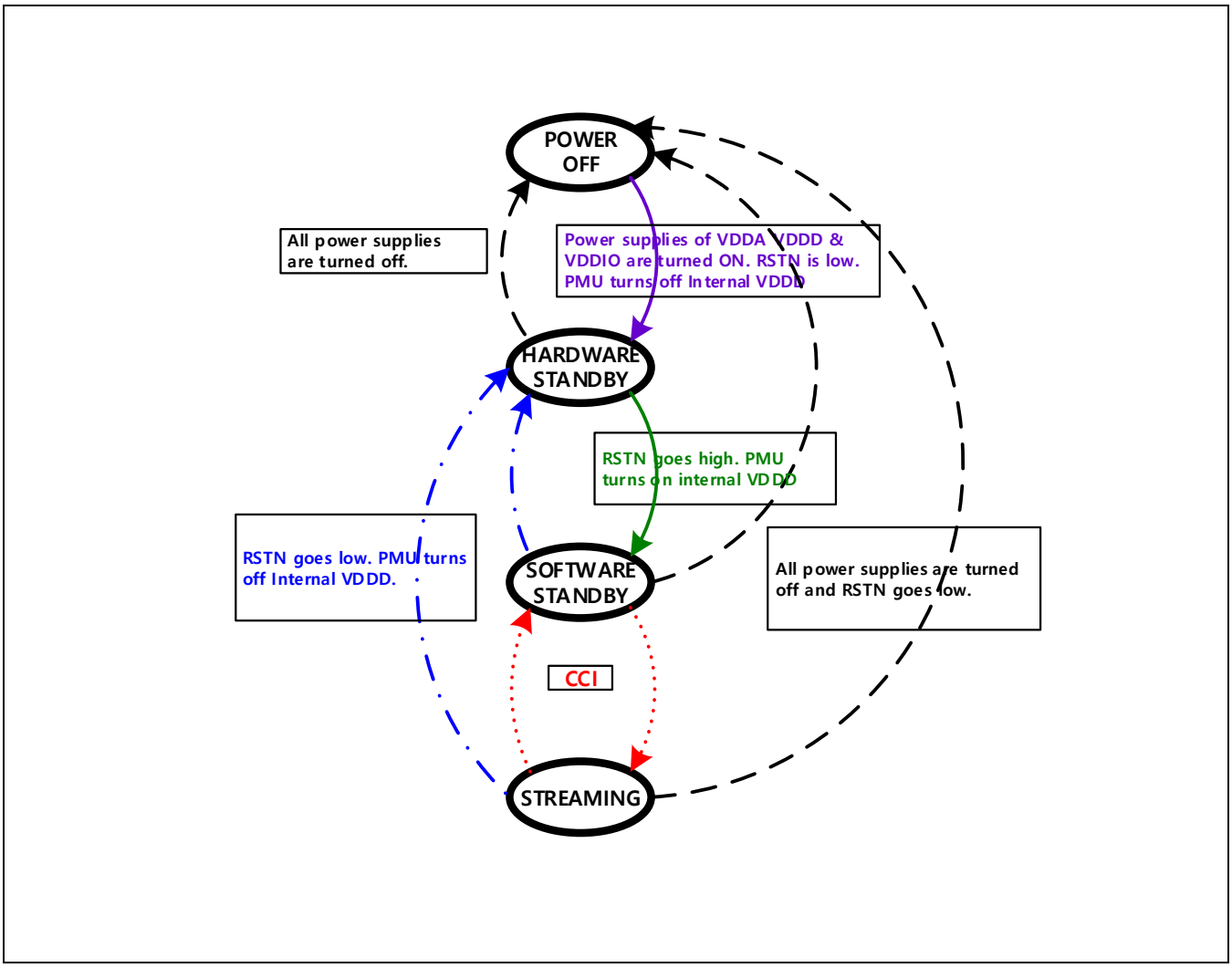

Figure 4 System State Diagram

Table 2 Operating Mode Summary

Power State	Description
Power-off	Power supplies are turned off.
Hardware standby	No communication with the sensor is possible.
Software standby	CCI communication with sensor is possible.
Streaming	The sensor module is fully powered and is streaming image data on the CSI-2 bus.

Table 3 describes the registers that control the operating mode of the camera module

Table 3 Operating Mode Registers

Start	Reset	Name	Type	Width	Description
0x0100	0x00	smiaRegs_rw_general_setup_mode_select	RW/SR	[0:0]	0 = Software Standby 1 = Streaming (Active Video)

3.2 Power-Up Sequence

The digital and analog supply voltages are recommended to be powered up in the following order. VDDD followed by VDDA. VDDIO can be powered up in any order.

On power up, RSTN (XSHUTDOWN) should be low when the power supplies are brought up, then the sensor module will go into hardware standby mode. As long as RSTN is low, the sensor module stays in hardware standby mode.

The assertion of RSTN and enabling MCLK clock ensures that the sensor module enters software standby mode and the CCI register values are initialized correctly to their default values.

When RSTN will go 'high', all PADs will exit from FAIL-SAFE mode, and switch to Normal operating mode.

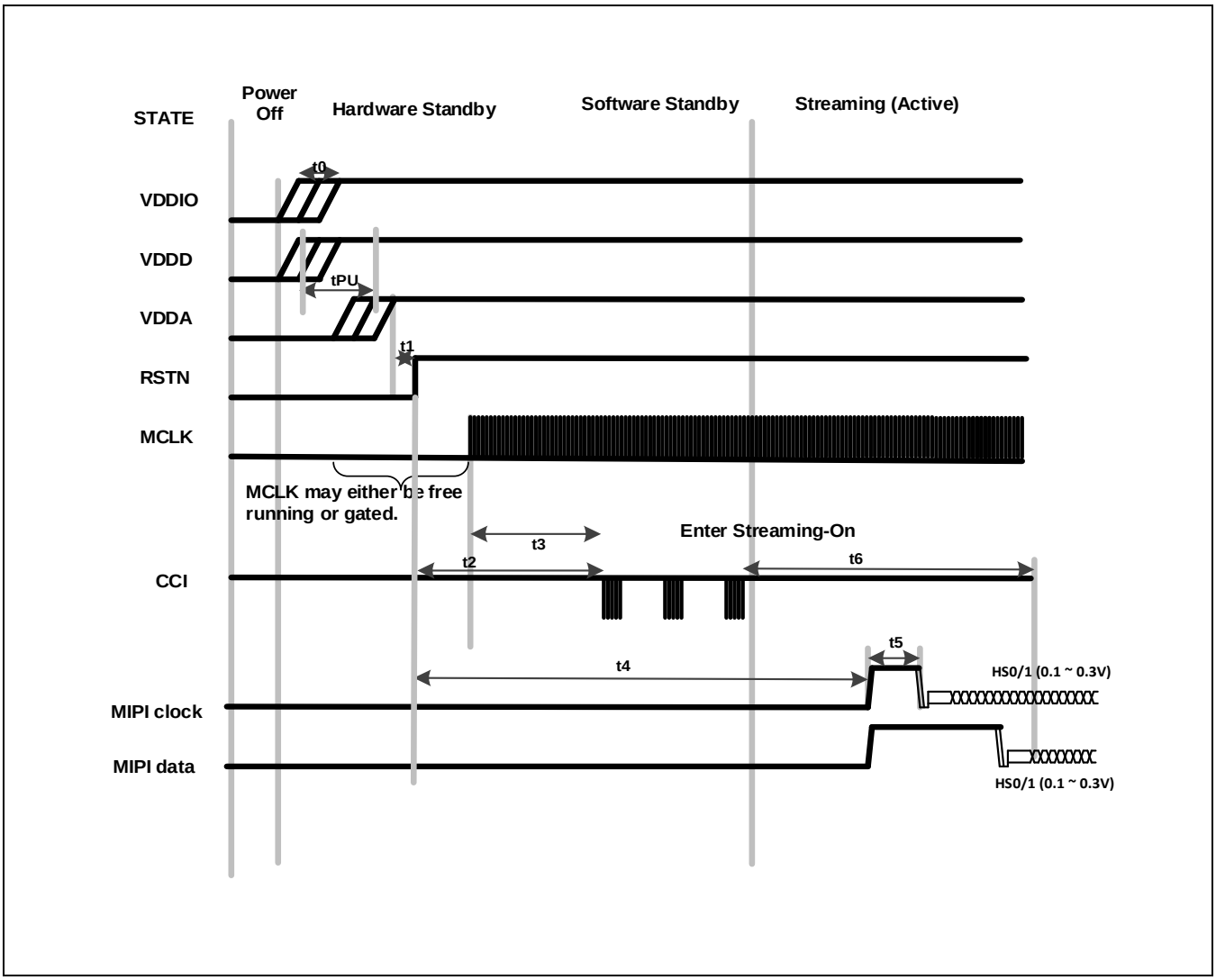

Figure 5 Power-Up Sequence

Table 4 Power-Up Sequence Timing Constraints

Constant	Label	Min.	Max.	Unit
VDDD/VDDIO rising time	t0	VDDD/VDDIO may rise in any order. The rising separation can vary from 0ns to indefinite. VDDA needs to follow the tPU guideline		ns
VDDD -> VDDA rising time	tPU	1		us
VDDA rising to RSTN (XSHUTDOWN) rising	t1	0.0	–	ns
RSTN (XSHUTDOWN) rising to first CCI transaction	t2	312050	–	MCLK cycles
Minimum No. of MCLK (EXTCLK) cycles prior to the first CCI transaction	t3	312050	–	MCLK cycles
DPHY initialization period (Wake-Up + PLL Lock Time)	t4	605	–	us
DPHY Clock Stable Time	t5	0.1	-	ms
Entering streaming mode-The first frame start sequence	t6	+ the delay according to the coarse integration time value	–	

3.3 Power-Down Sequence

The digital and analog supply voltages are recommended to be powered down in the following order. VDDA followed by VDDD. VDDD/VDDIO can be powered down in any order.

Similar to the power-up sequence, the MCLK (EXTCLK): input clock may be either gated or continuous.

If CCI command to exit streaming is received when it outputs a frame of valid active data, then the sensor module waits for the frame end code before entering software standby mode. Frame end code comes either after all frame pixels are transmitted or during the frame when next line transmission is completed based on a configuration register. For more information, refer to S5KJNSSQ33 Application Notes.

If the CCI command to exit streaming mode is received during the inter frame time, then the sensor module must enter software standby mode immediately.

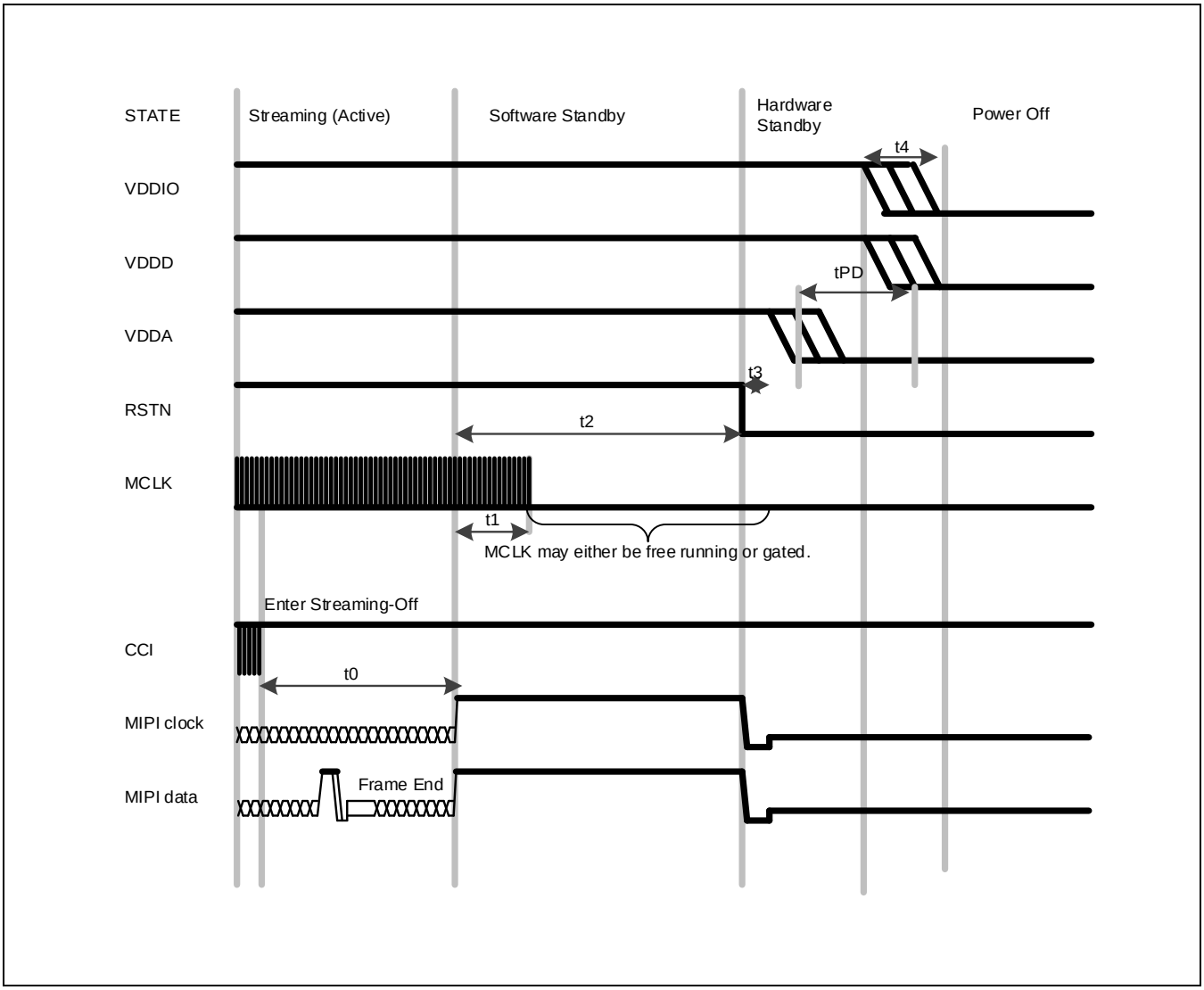

Figure 6 Power-Down Sequence

Table 5 Power-Down Sequence Timing Constraints

Constant	Label	Min.	Max.	Unit
Enter Software Standby CCI command- Device in Software Standby mode	t0	If outputting a frame of MIPI, the data waits for the MIPI frame end code before entering software standby; otherwise enter software standby mode immediately.		–
Minimum number of MCLK (EXTCLK) cycles after the last CCI transaction or MIPI frame end code.	t1	512	–	MCLK cycles
Last CCI Transaction or MIPI frame end code - RSTN (XSHUTDOWN) falling	t2	512	–	
RSTN (XSHUTDOWN) falling to VDDD or VDDA falling	t3	0.0	–	ns
VDDA falling -> VDDD falling	tPD	1		us
VDDD/VDDIO falling time	t4	VDDD/VDDIO may fall in any order. The rising separation can vary from 0 ns to indefinite		ns

3.3.1 Exit streaming preliminary condition

The CCI command to exit streaming must be issued only after sensor module entered streaming mode, therefore, after issuing enter streaming mode CCI command, user must verify frame counter value changed from 0xFF to a value greater than 0x0, before issuing exit streaming mode CCI command:

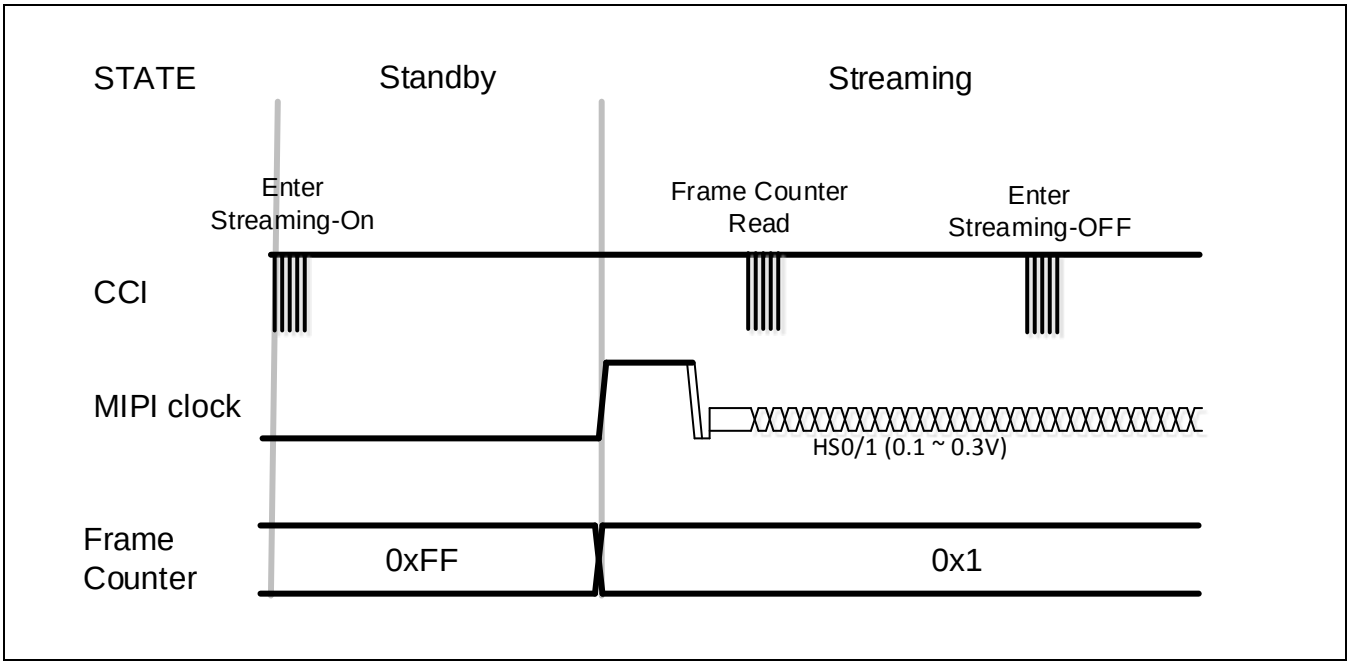

Figure 7 Exit Streaming preliminary condition

Table 5.1 - describes the parameters to define the various processes of handling last frame before entering the software reset.

Table 6 Frame Count register

Timing Transition Type	Setting
api_rd_general_frame_count	0xFF = Currently in Standby state
	0x0 = On reset and during boot sequence until first stand-by
	0x1-0xFE = Incremental counter (with wrap-around)

3.4 Software Standby Mode Sequence

Entering software standby mode is the same as entering hardware standby mode but without RSTN (XSHUTDOWN) assertion to low.

Table 7 describes the parameters to define the various processes of handling last frame before entering the software reset.

Table 7 Abort Frame Timing Transition Options upon Entering SW Reset

Timing Transition Type	Setting
abort_timing_on_sw_stby	0 = Abort timing Immediately, even during read out.
	1 = Abort timing after read out ends
	2 = Abort timing on end of frame.

4 Control Interface

S5KJNSSQ33 control is done using register writes.

S5KJNSSQ33 is configured using the I2C_SPI_N_SEL pin and controlled using Camera Control Interface (CCI) or Serial Peripheral Interface (SPI).

Table 8 SPI/I2C PAD Sharing

SPI	I2C
SDI	SDA
SCK	SCL
XCE	I2C_ID (LSB of slave ID selector)
SDO	–
	I2C_ID1 (MSB of slave ID selector)
I2C_SPI_N_SEL	

4.1 Camera Control Interface (CCI)

S5KJNSSQ33 supports Camera Control Interface (CCI), which is an I2C fast-mode compatible interface for controlling the transmitter. S5KJNSSQ33 always acts as a slave in CCI bus. CCI can handle several slaves in the bus, but multi-master mode is not supported. Typically, only receiver and transmitter are connected to CCI bus. This ensures a pure S/W implementation.

CCI is separate from the system I2C bus, but I2C compatibility ensures that it can connect the transmitter to the system I2C bus. CCI is a subset of I2C protocol, including the minimum combination of obligatory features for the I2C slave device specified in I2C specification. Transmitters complying with CCI specification are connected to the system I2C bus. However, to ensure that I2C masters do not utilize these I2C features that are not supported in transmitters complying with CCI specification. Each transmitter conformed to CCI specification have additional features implemented to support I2C.

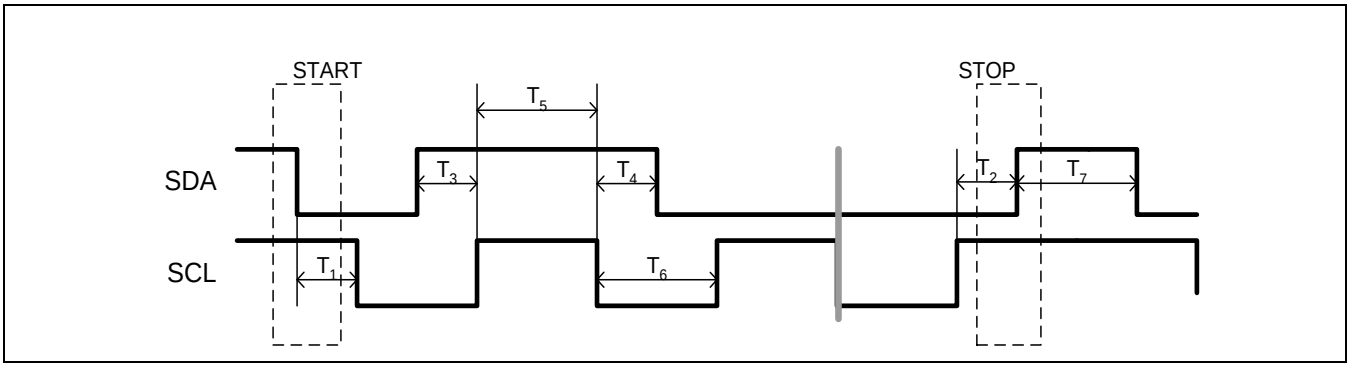

Figure 8 Timing Diagram of CCI

Table 9 I2C Standard Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	100	kHz
Hold time for START condition	T_1	4.0	–	µs
Setup time for STOP condition	T_2	4.0	–	
Data setup time	T_3	250	–	ns
Data hold time	T_4	0	3.45	µs
High period of the SCL clock	T_5	4.0	–	
Low period of the SCL clock	T_6	4.7	–	
Bus free time between STOP and START conditions	T_7	4.7	–	
Rise time for both SDA and SCL signals	–	–	1000	ns
Fall time for both SDA and SCL signals	–	–	300	

Table 10 I2C Fast Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	400	kHz
Hold time for start condition	T_1	0.6	–	µs
Setup time for stop condition	T_2	0.6	–	
Data setup time, external clock (MCLK) above 12.8MHz	T_3	0.1	–	µs
Data setup time, external clock (MCLK) below 12.8MHz		0.6	–	
Data hold time	T_4	0	0.9	µs
High period of the SCL clock	T_5	0.6	–	
Low period of the SCL clock	T_6	1.3	–	
Bus free time between stop and start conditions	T_7	1.3	–	
Rise time for both SDA and SCL signals	–	–	300	ns
Fall time for both SDA and SCL signals	–	–	300	

NOTE: A Fast-mode I2C-bus device can be used if the external clock is above 14 MHz

Table 11 I2C Fast Mode plus (FM+) Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	1	MHz
Hold time for start condition	T_1	0.26	–	µs
Setup time for stop condition	T_2	0.26	–	
Data setup time, external clock (MCLK) above 24MHz	T_3	0.05	–	µs
Data setup time, external clock (MCLK) between 12.8-24MHz		0.1	–	
Data setup time, external clock (MCLK) below 12.8MHz		0.6	–	
Data hold time	T_4	0	–	µs

Parameter	Symbol	Min.	Max.	Unit
High period of the SCL clock	T_5	0.26	–	
Low period of the SCL clock	T_6	0.5	–	
Bus free time between stop and start conditions	T_7	0.5	–	
Rise time for both SDA and SCL signals	–	–	120	ns
Fall time for both SDA and SCL signals	–	–	120	

NOTE: A Fast-mode Plus I2C-bus device can be used if the external clock is above 16 MHz

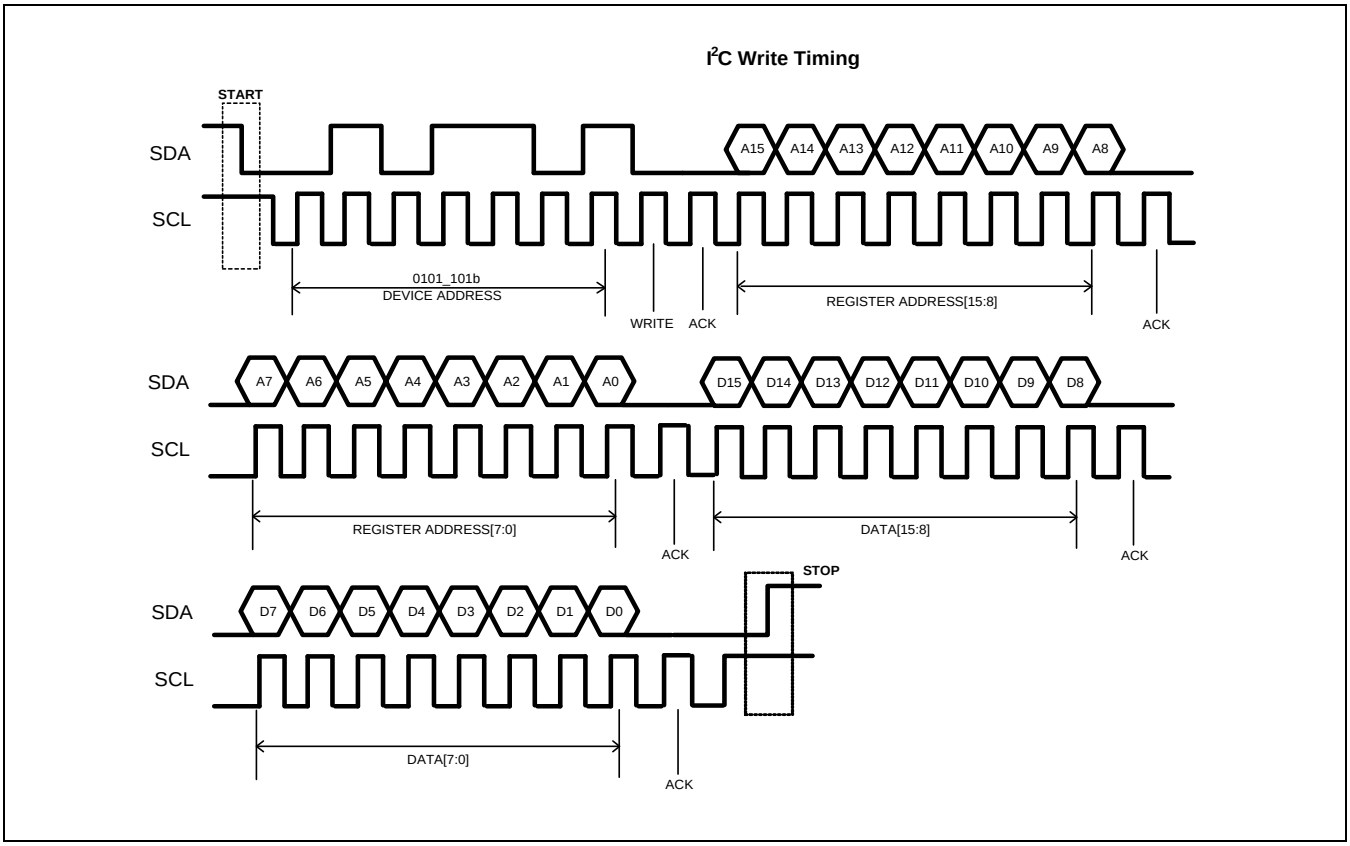

Figure 9 Timing Diagram of CCI Write

NOTE: The device address can be changed by pin configuration of XCE and I2C_ID1 pads as described in Table 12.

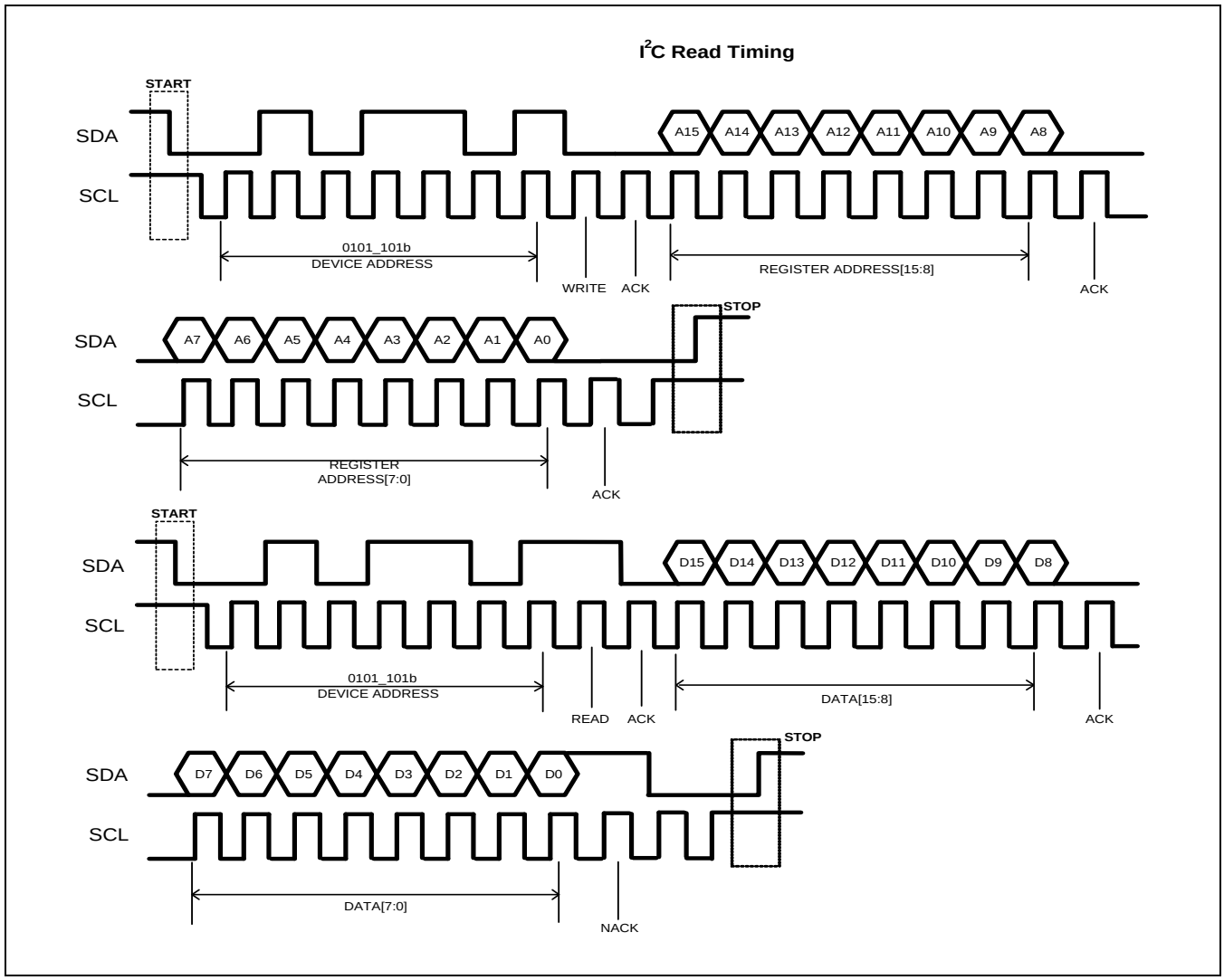

Figure 10 Timing Diagram of CCI Read

NOTE: The device address can be changed by pin configuration of XCE and I2C_ID1 pads as described in Table 12

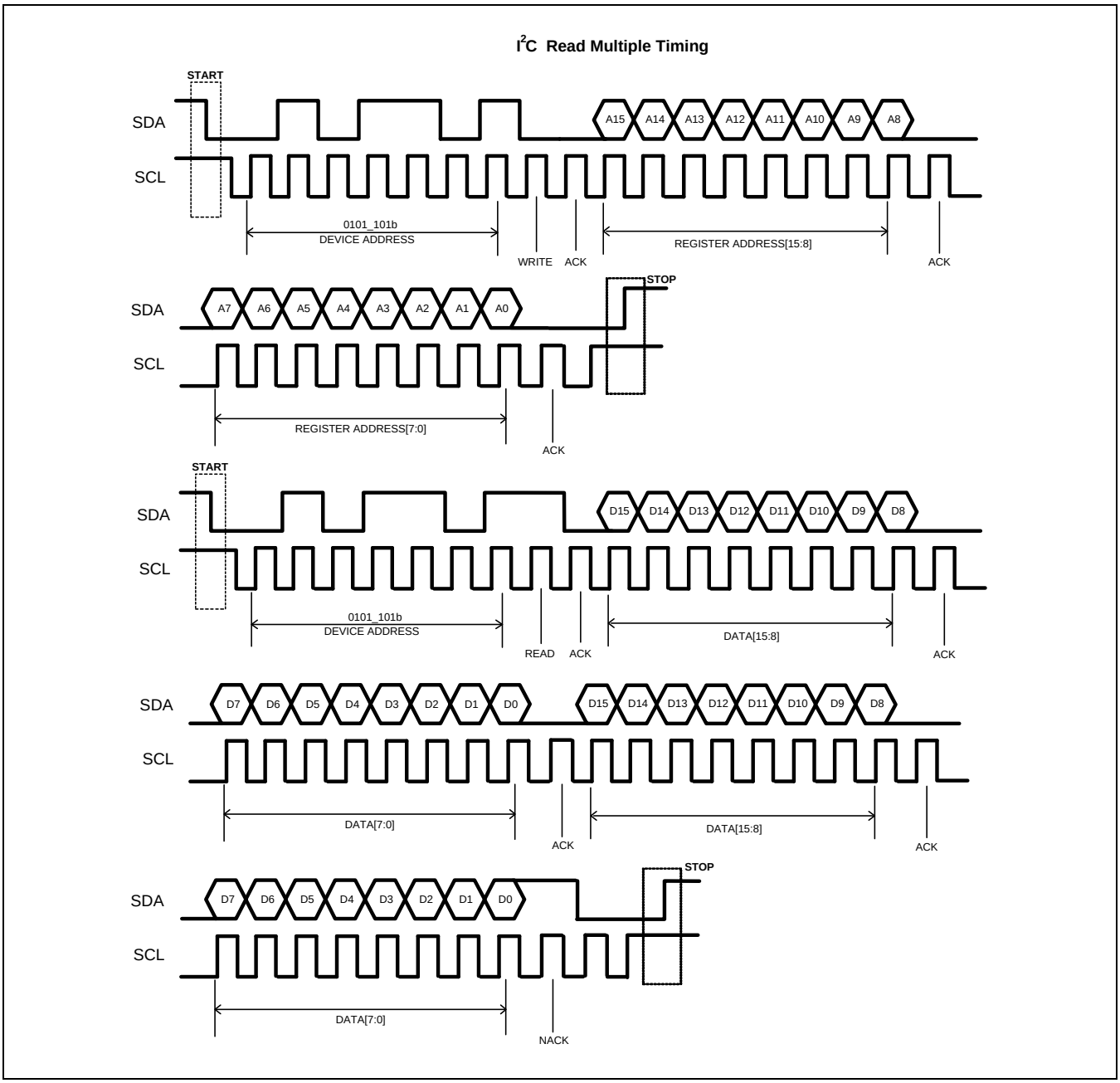

Figure 11 Timing Diagram of Multiple CCI Read

NOTE: The device address can be changed by the pin configuration of XCE and I2C_ID1 as described in Table 12.

It can configure up to four I2C slave addresses using XCE and I2C_ID1 pads.

Table 12 I2C ID Address (XCE and I2C_ID1 Pads)

{I2C_ID1,XCE}	Slave Address (7-bit + Read Mode)	Slave Address (7-bit + Write Mode)	Comment
2'b00	0010_0001b/21h	0010_0000b/20h	Address 1
2'b01	0101_1011b/5Bh	0101_1010b/5Ah	Address 2
2'b10	0111_1011b/7Bh	0111_1010b/7Ah	Address 3
2'b11	1010_1101b/ADh	1010_1100b/ACh	Address 4

4.2 SPI Control Interface

S5KJNSSQ33 can use the SPI interface for communicating with control registers.

Figure 4-1 illustrates the SPI control interface.

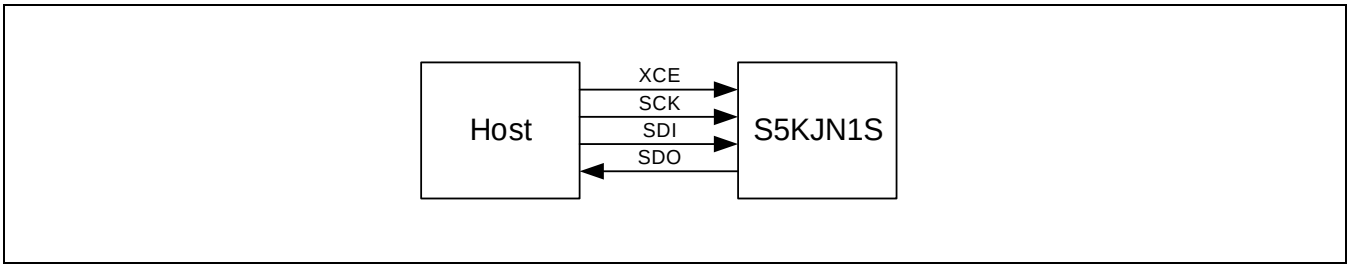

Figure 12 SPI Control Interface

Table 13 describes SPI signals.

Table 13 SPI Signals

Pin Name	Description
XCE	Serial communication enable input
SCK	Serial communication clock input
SDI	Serial data input
SDO	Serial data output

If it is not necessary to read the control registers and chip ID, the SDO pad can be left unconnected.

The SPI control interface implemented in S5KJNSSQ33 is described in detail in the Section 4.2.1, 4.2.2 and 4.2.3.

4.2.1 SPI Timing Definitions

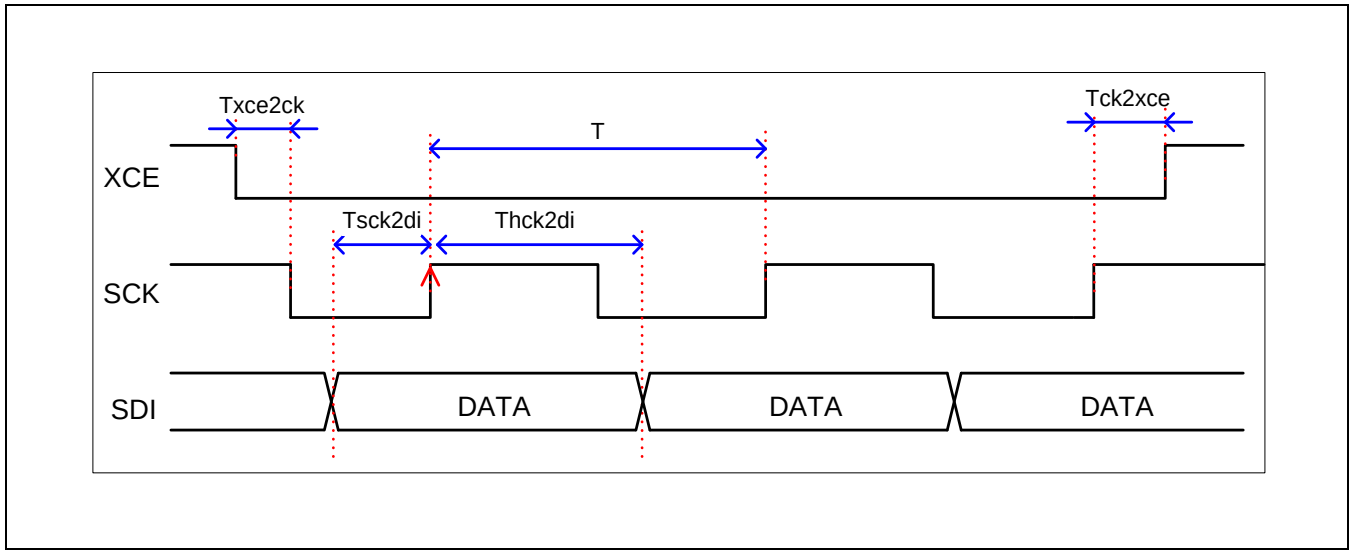

Figure 13 Timing Diagram of SPI Write Mode 11

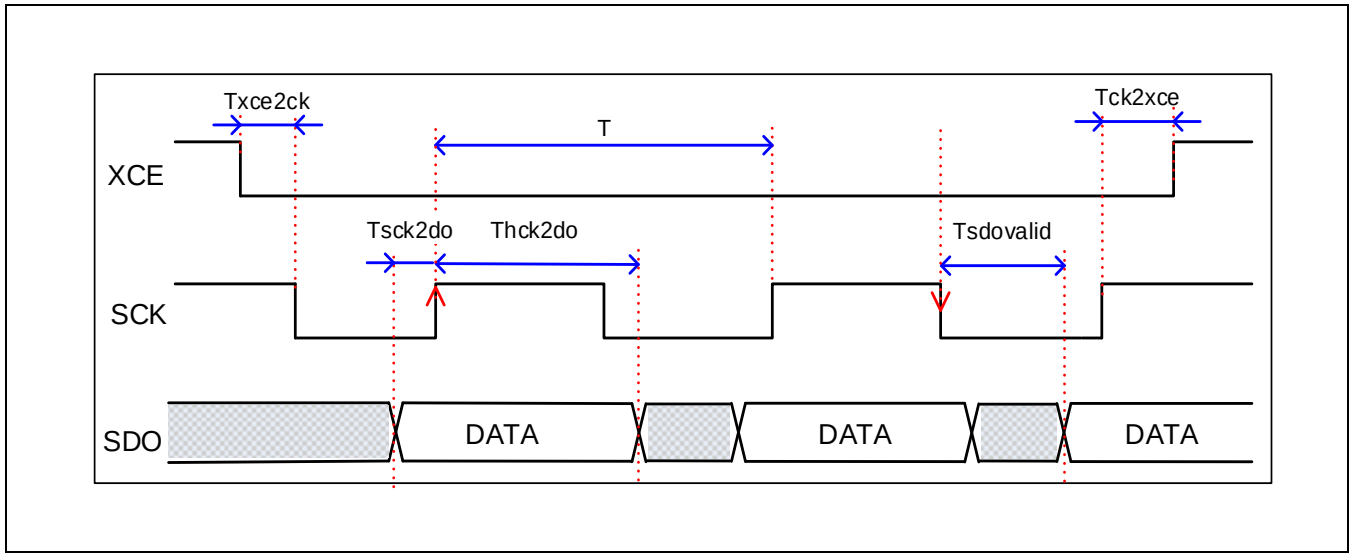

Figure 14 Timing Diagram of SPI Read Mode 11

Table 14 SPI Write/Read Timing Specification

Description	Symbol	Min.	Typ.	Max.	Unit
MCLK (external clock) frequency	Fext	12	–	64	MHz
SPI clock frequency	F (1)	–	–	Fext/3	
	F (2)	–	–	20	
SPI clock period	T	1/F	–	–	nSec
SPI clock duty cycle	Tdc	45	–	55	%
XCE negedge to SCK edge	Txce2ck	T	–	–	nSec
SCK posedge to XCE edge	Tck2xce	2T	–	–	
SCK to SDI setup time	Tsck2di	7	–	–	
SCK to SDI hold time	Thck2di	5	–	–	
SDO data valid time	Tsdovalid	4.5	-	12.5	
SCK to SDO setup time	Tsck2do	T/2-20	–	–	
SCK to SDO hold time	Thck2do	T/2	–	–	

NOTE:

1. External clock is used.
2. PLL stable. Internal system clock set to Max. 60 MHz

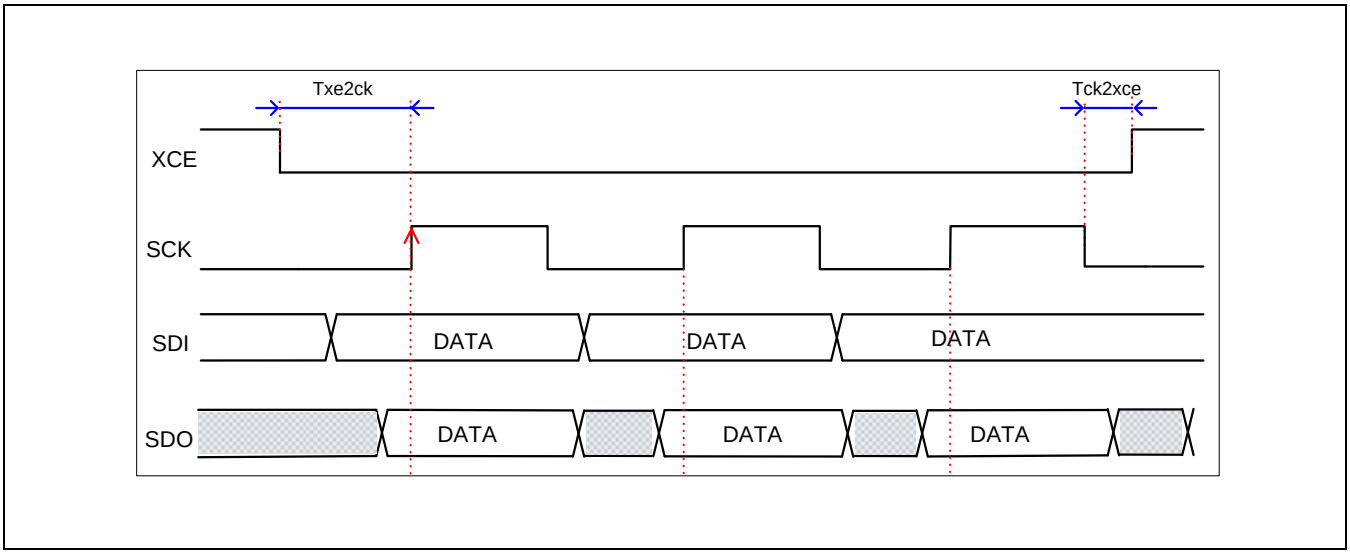

Figure 15 Timing Diagram of SPI Write/Read Mode 00

4.2.2 SPI Sequences

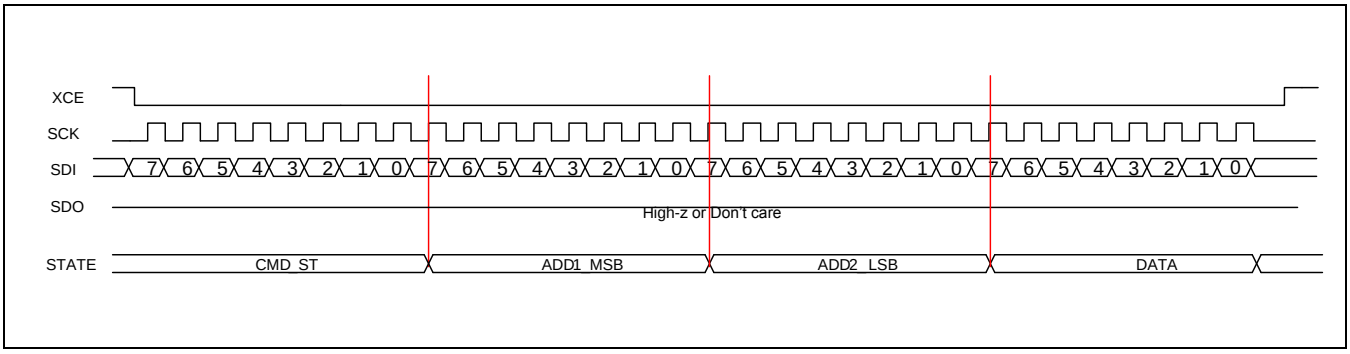

Figure 16 SPI Write Sequence (1 Cycle)

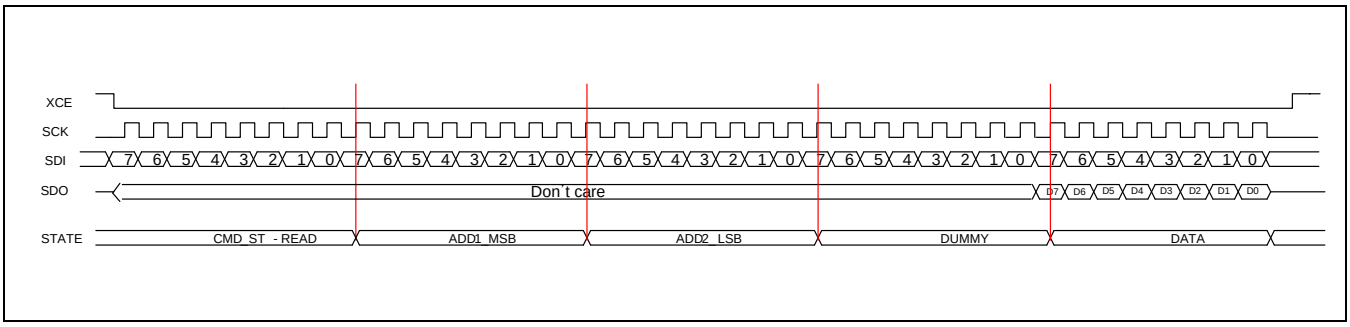

Figure 17 SPI Read

5 Functional Features

5.1 Block Diagram

S5KJNSSQ33 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip Phase-Locked Loop (PLL) to generate all internal clocks from a single master input clock running between 12 MHz and 64 MHz. Dedicated PLL generates the output interface clocks for maximum flexibility in interface frequency and avoiding EMI.

The block diagram of the sensor is shown in *Figure 18*.

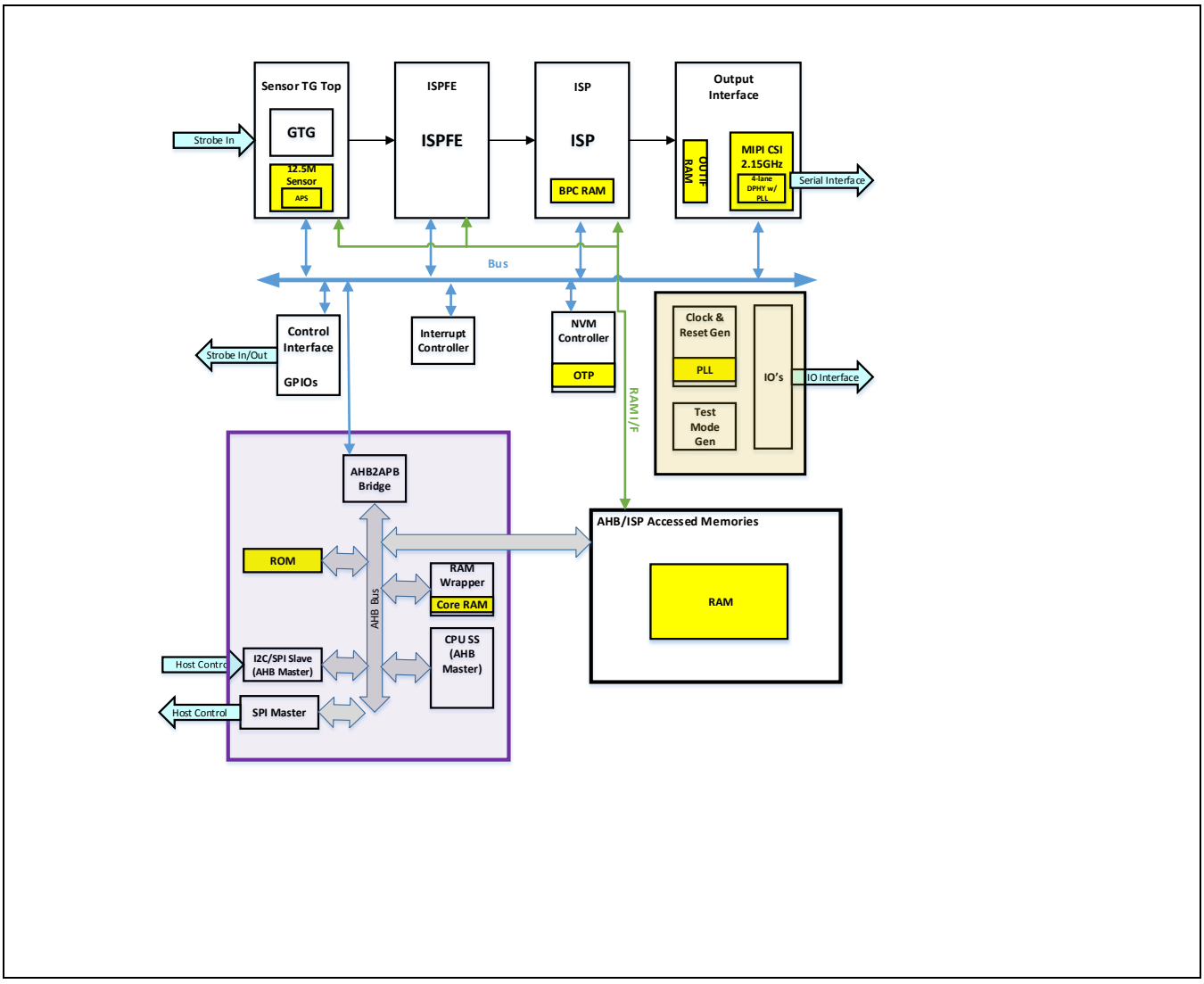

Figure 18 Function Block Diagram

The image sensor has an on-chip ADC. A column parallel ADC scheme is used for low-power analog processing.

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate these noise components, a Correlated Double Sampling (CDS) circuit is used before converting the analog signal to digital.

The output from the ADC is a 10-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain, which provides further data path corrections and applies digital gain.

The digital processing chain performs frame black level recovery, compensation for various analog circuit variations, and non-uniform pixel levels. These compensations are more flexible in allowing different compensation for each pixels type and exposure level.

S5KJNSSQ33 has a deterministic pattern generator and a MIPI CSI-2 frame formatter with embedded line support.

The sensor is interfaced using a set of control and status registers that is used to control many aspects of the sensor behavior, including frame size, exposure, and gain setting. These registers are accessed through a CCI or SPI interface.

5.2 Pixel Array Addresses

Addressable pixel array is defined as the pixel address range to be read. The addressable pixel array is assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by the x_addr_start, y_addr_start, x_addr_end, y_addr_end, x_output_size, and y_output_size registers.

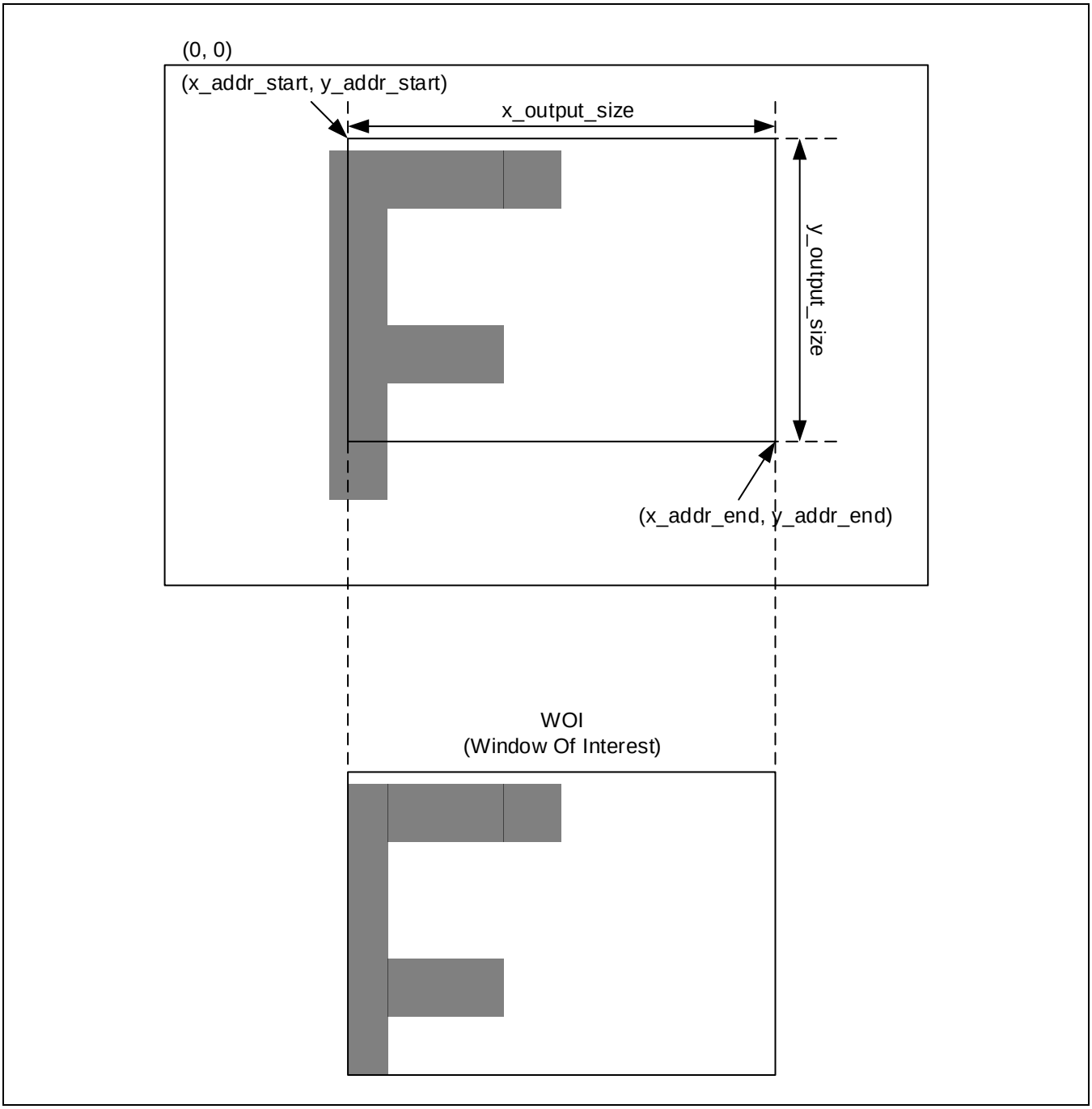

Figure 19 Window of Interest on Pixel Array

5.3 TetraCell

Enabling the summation changes the output order of S5KJNSSQ33.

5.3.1 Output Mode

S5KJNSSQ33 supports summing output mode

- Summing output mode – 12.5 MP Bayer output that is the result of 4-pixel summation

Summing Output Mode

In the summation mode, sensor averages the adjacent same color pixels. So, output re-ordering is not needed to keep the Bayer array order.

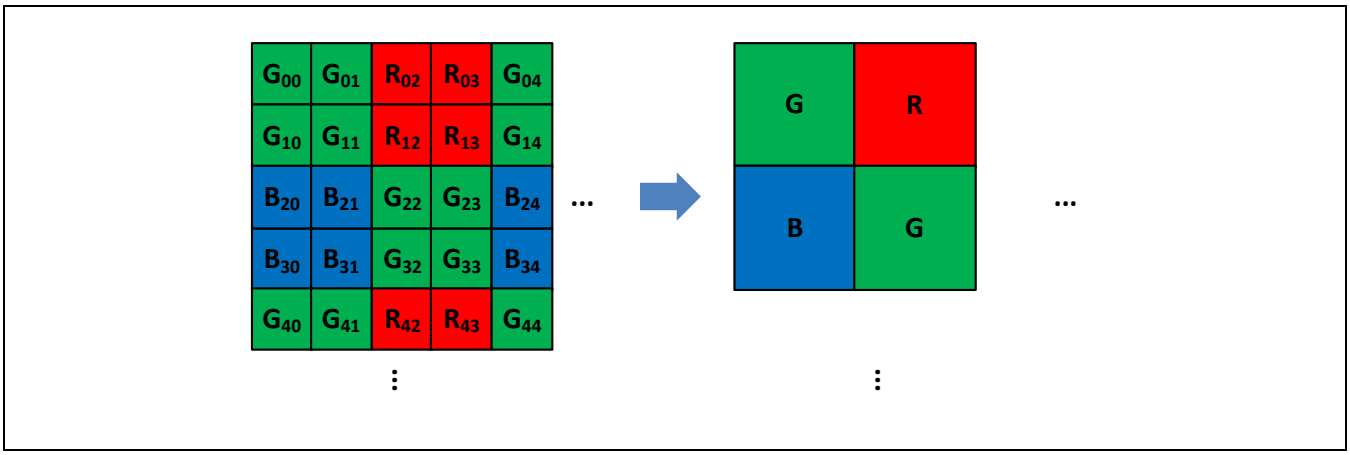

Figure 20 Summation Output Mode

5.4 Horizontal Mirror and Vertical Flip

The pixel data is normally read out from left to right in horizontal direction and from top to bottom in vertical direction. By changing the mirror/flip mode, the read-out sequence can be reversed, and the resulting image can be flipped as a mirror image. Pixel data is then read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. Horizontal mirror and vertical flip mode are programmed by image orientation register.

The sensor module supports following four possible pixel readout orders according to the directions of pixel readout and line readout:

- Standard readout
- Horizontally mirrored readout
- Vertically flipped readout
- Horizontally mirrored and vertically flipped readout

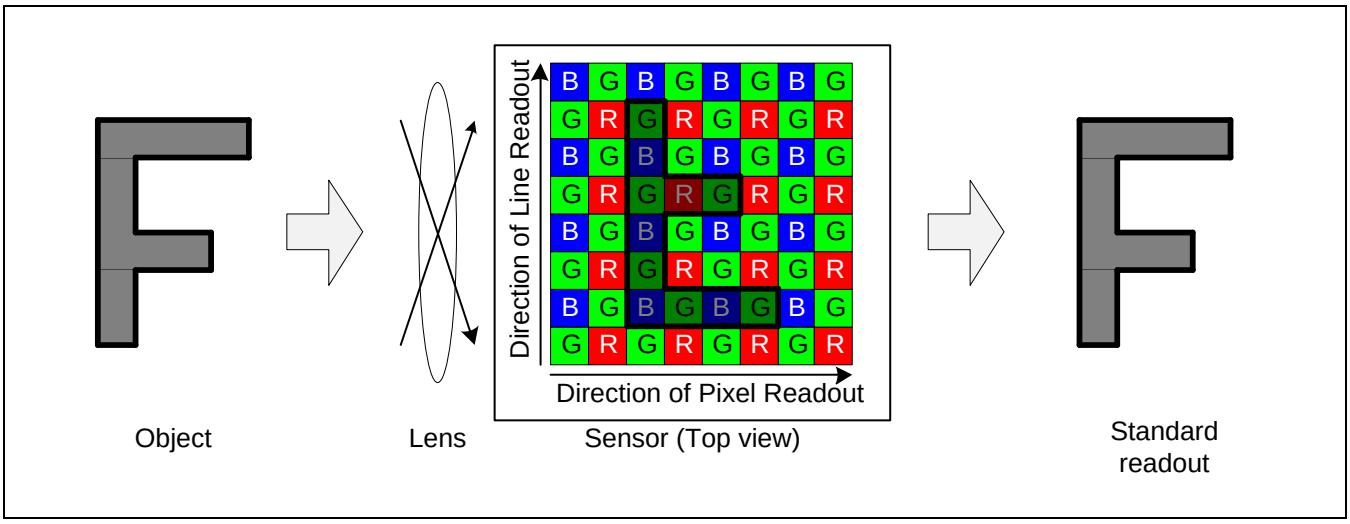

Figure 21 Object, Sensor and displayed image in Standard Readout

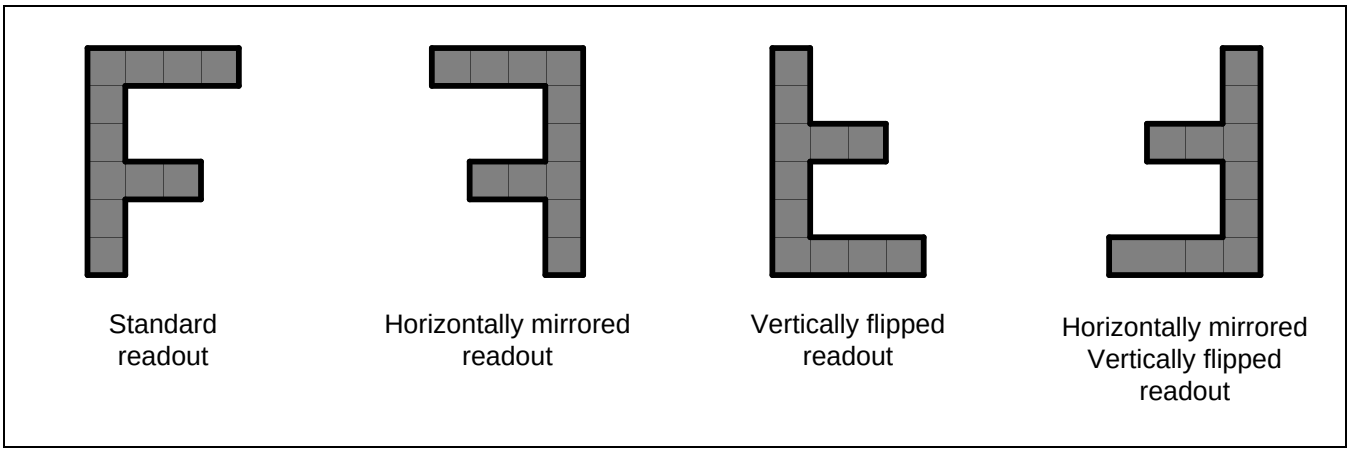

Figure 22 Four readout orders and displayed images

5.5 Frame Rate Control

Line rate and frame rate are changed by varying the size of the virtual frame. The width and depth of virtual frame are controlled by line_length_pck and frame_length_lines registers. Horizontal and vertical blanking times (horizontal blanking time is given by line_length_pck-x_output_size, vertical blanking time is given by frame_length_lines-y_output_size) should meet system requirements.

Frame rate = vt_pix_clk/(frame_length_lines × line_length_pck)

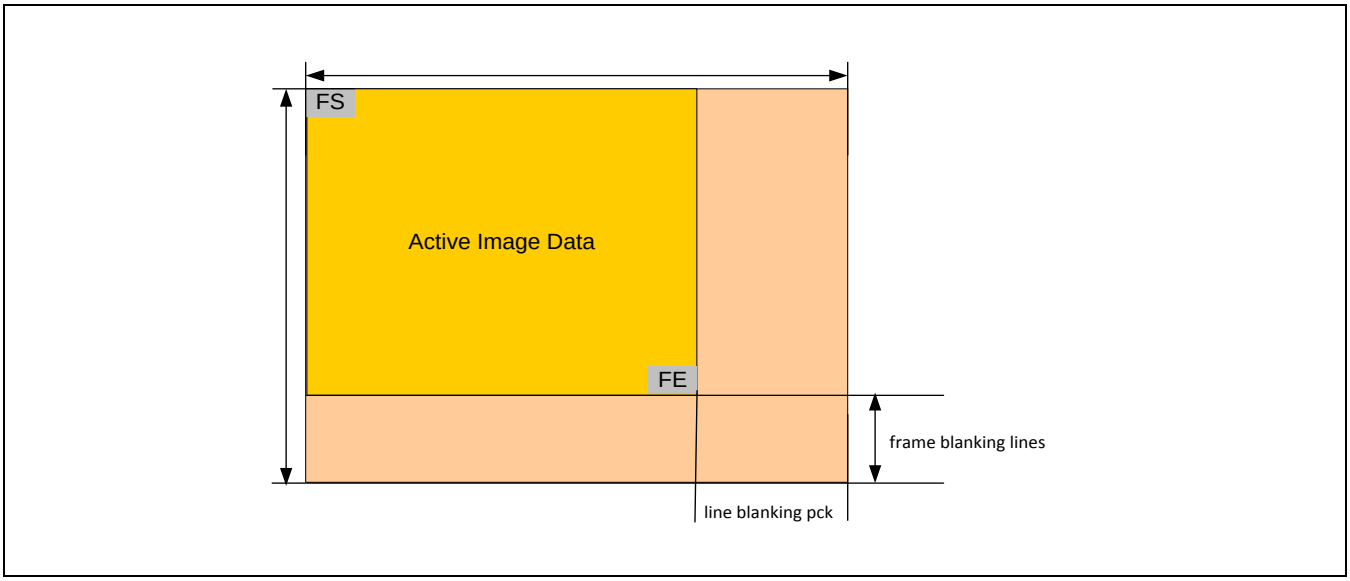

Figure 23 Virtual Frame Format Example

5.5.1 Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by the shutter operation. During shutter operation, amount of time (integration time) is determined by column step integration time control register (fine_integration_time) and line step integration time control register (coarse_integration_time). Total integration time of sensor module is calculated using the following formula.

Total_integration_time = {coarse_integration_time × line_length_pck + fine_integration_time} × pclk period[sec]

5.5.2 Functional Operation Modes

S5KJNSSQ33 can support a wide range of operation modes.

Operation mode is function of several mode parameters such as:

- Interface bandwidth
- Image requested quality
- HW limitations (minimal H/V-blank, delay of blocks)
- Requested sensor output size and sensor operation mode
- CIS output size and number of bits per pixel for example, RAW 10
- Required VBlank time
- Power consumption limitations for example, using single PLL, limited MIPI lanes, and system low-power modes

Table 15 describes typical optional operation modes and related typical settings.

Table 15 Typical Functional Operation Modes

Mode	Frame Rate	Crop, Ratio	CIS Output		Binning		Comments	AF
			H	V	H	V		
Binning(12.5 MP)	30 fps	NO, 4:3	4080	3072	2	2	Summation Mode	Note 1
UHD	60fps	HVCrop, 16:9	3840	2160	2	2	Summation Mode + Crop	Note 1
FHD	240fps	HVCrop, 16:9	1920	1080	4	4	Summation Mode + Average Mode + Crop	Note 1
HD	240fps	HVCrop, 16:9	1280	720	4	4	Summation Mode + Average Mode + Crop	Note 1

Note 1: Support both PDAF tail-mode and PDAF Implant mode

5.6 PLL and Clock Generator

S5KJNSSQ33 clock system uses system PLL, system clock dividers, output PLL, and output clock dividers to generate all internal clocks from a single master input clock running between 12 MHz and 64 MHz.

System clocks may be generated by the output PLL. In this case the system PLL will be powered-down and overall system power gets reduced. The maximum effective VCO of output PLL for MIPI transmission is 2.15 GHz. The maximum VCO of output PLL for system requirements is divided by 2 (1075 MHz).

The dedicated system PLL is used for maximal flexibility in interface frequency and for EMI avoidance. The maximum system PLL VCO frequency is 1200 MHz.

Clock dividers are used to generate all system clocks from one or two PLL sources.

Charge pump and ADC clock are used for A/D conversion circuits. Pixel clock and pixel clock/2 are used for pixel processing and sensor control. Bit clock and output clock are set according to the required output rate.

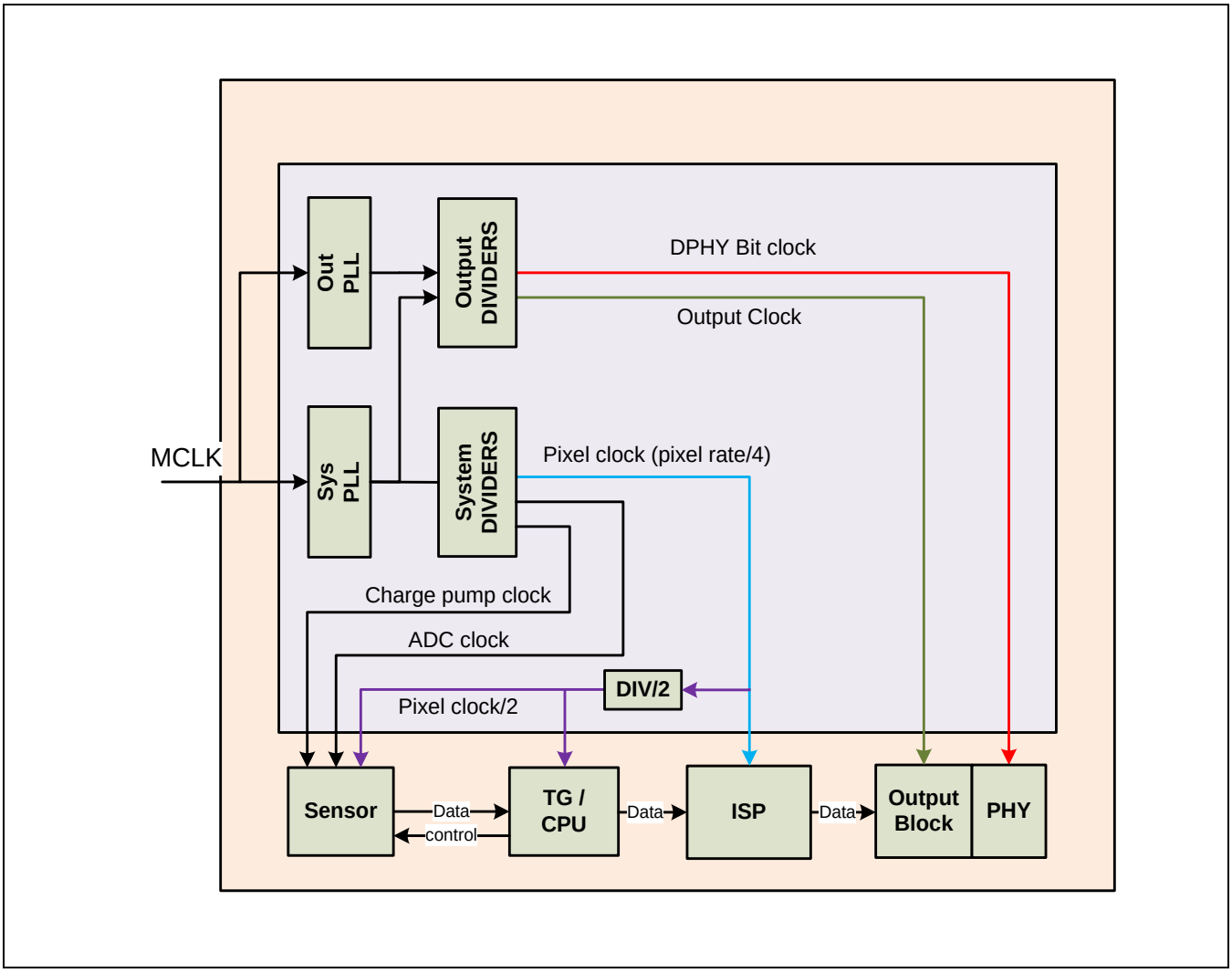

Figure 24 Clock System Block Diagram

5.6.1 Clock Relationships

The host sets dividers and multipliers and also provides external input clock (with values varying between 12 MHz and 64 MHz) to get required video timings and output pixel clocks.

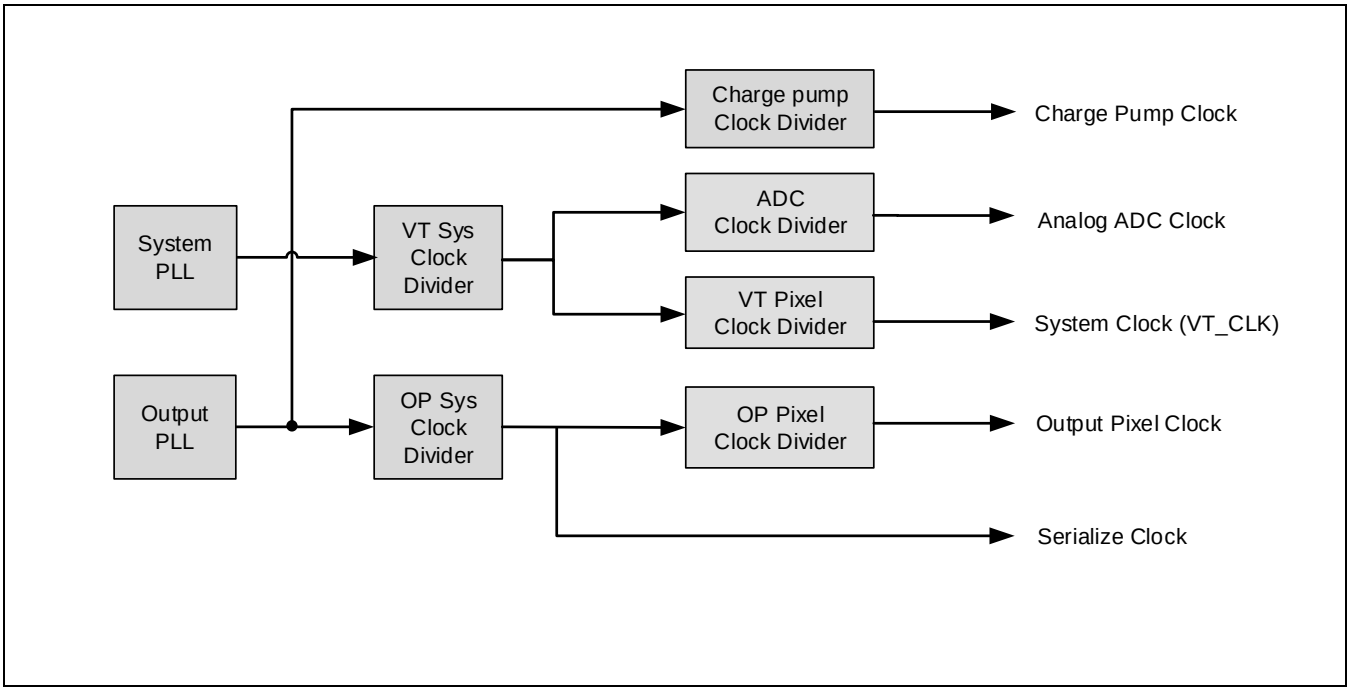

Figure 25 Clock Relationships

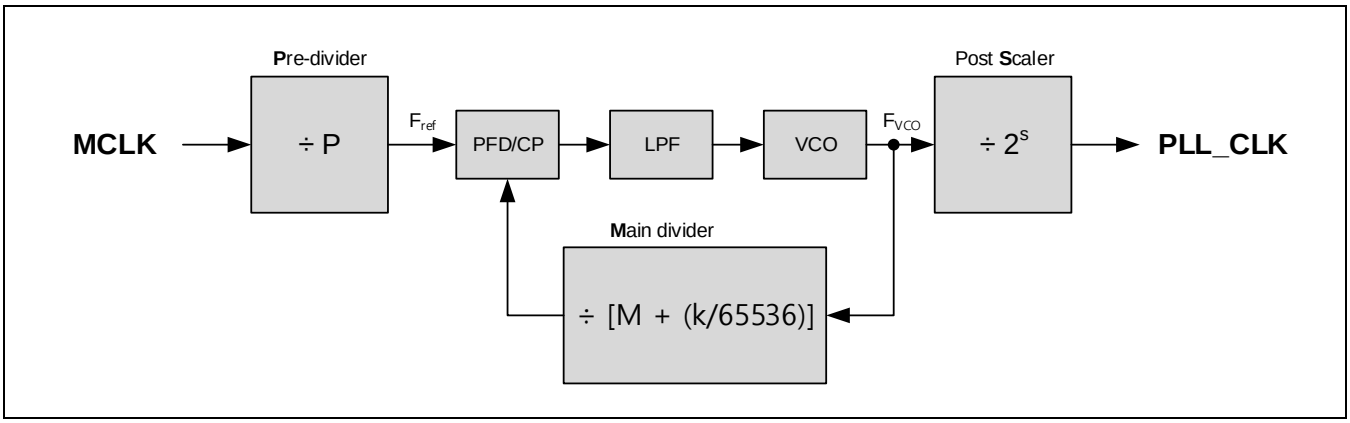

Figure 26 PLL Frequency Synthesis

$$PLL\_CLK = MCLK \times \frac{(M + k/65536)}{P} \times \frac{1}{2^S}$$

NOTE: Default value of k is 0

Table 16 PLL Component Output Frequency

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input frequency range	12	–	64	MHz	EXTCLK frequency range
System PLL reference frequency range	6	–	12	MHz	Output of system PLL pre-divider (Fref)
System PLL VCO frequency range	640	–	1200	MHz	Output of system PLL multiplier VCO oscillation range (Fvco)
System PLL output frequency range	40	–	1200	MHz	Output of system PLL post scaler. Minimum value is only for testing purpose. (5 > S ≥ 0)
Output PLL reference frequency range	6	–	12	MHz	Output of output PLL pre-divider (Fref)
Output PLL VCO frequency range	600	–	1075	MHz	Output of output PLL multiplier VCO oscillation range (Fvco). Effective frequency for MIPI transmission is x2 faster
Output PLL output frequency range	37.5	–	1075	MHz	Output of output PLL post scaler. Minimum value is only for testing purpose. (5 > S ≥ 0). Effective frequency for MIPI transmission is x2 faster

NOTE: For more information about the PLL and clock system control, refer to the S5KJNSSQ33 Application Notes.

5.6.2 Master Clock Waveform Diagram

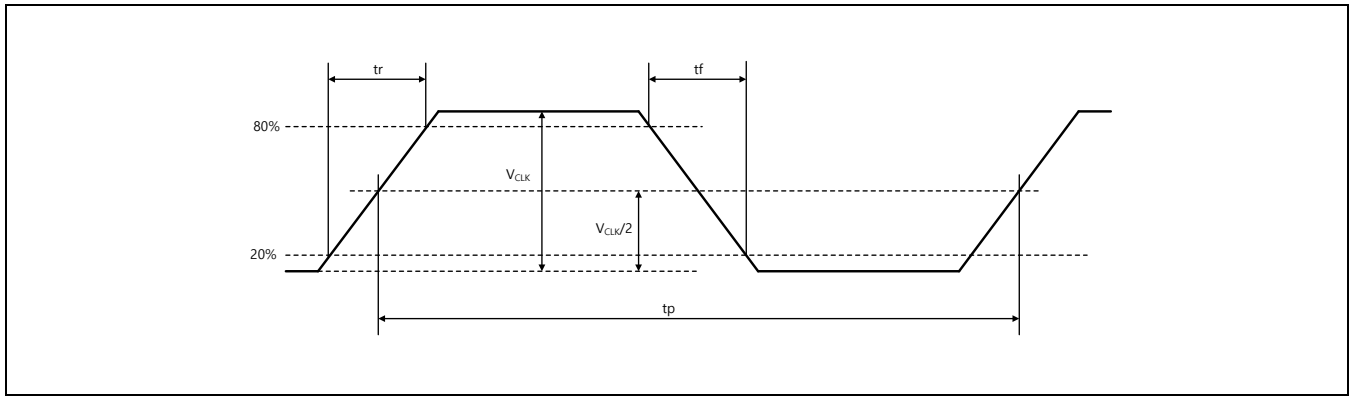

Figure 27 Master Clock Waveform Diagram

MCLK is the input clock to S5KJNSSQ33 sensor, also referred as EXTCLK (external clock).

Table 17 MCLK timing spec

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
MCLK clock frequency	MCLK	12	–	64	MHz	Note
MCLK period	tp	15.625	–	83.33	ns	–
MCLK rise/fall time	tr/tf	–	–	10		–
MCLK period jitter(peak-to-peak)	Tjitter	–	–	600	ps	–

Note: Min MCLK is 16MHz at I2C Fast Mode Plus (FM+)

5.7 Gain Control

5.7.1 Analog Gain Control

Analog gain can be calculated by the following equation:

$$gain = \frac{x}{0x20}$$

NOTE: In S5KJNSSQ33, analog gain is global; there is no per-channel gain. $gain = \frac{x}{32}$
Gain is supported up to X64.

S5KJNSSQ33 supports analog gain up to 64 times only in 12.5MP/UHD @ 30 fps (Bayer) and FHD/HD @ 240 fps (Bayer).

We can also control the divider (default value is 0x20) and multiply it by 2^N.

N is controlled by the following register.

Table 18 Analog Gain Examples

Gain Value	analog_gain_code_XXX Register Value
X1	0x0020
X2	0x0040
X3	0x0060
X8	0x0100
X10	0x0140
X12	0x0180
X16	0x0200
X32	0x0400
X64	0x0800

5.7.2 Digital Gain Control

This block handles digital gains.

Digital gain registers are coarse and support fractional gain of 1/256 scale.

Table 19 Digital Gain Examples

Gain Value	digital_gain_code_XXX Register Value
X1	0x0100
X2	0x0200
X3	0x0300
X8	0x0800
X16	0x1000

5.8 Embedded Line

S5KJNSSQ33 is configured to generate an embedded MIPI header with frame information.

5.9 NVM OTP Memory

The OTP memory module is a non-volatile OTP memory module. This module saves unique data to each chip at the production stage.

OTP memory is used to store the following information:

- Chip ID data – Production history data is stored during die sorting
- 512 bytes for users

5.10 Dual camera input Sync

Dual Camera support is also provided with the S5KJNSSQ33.

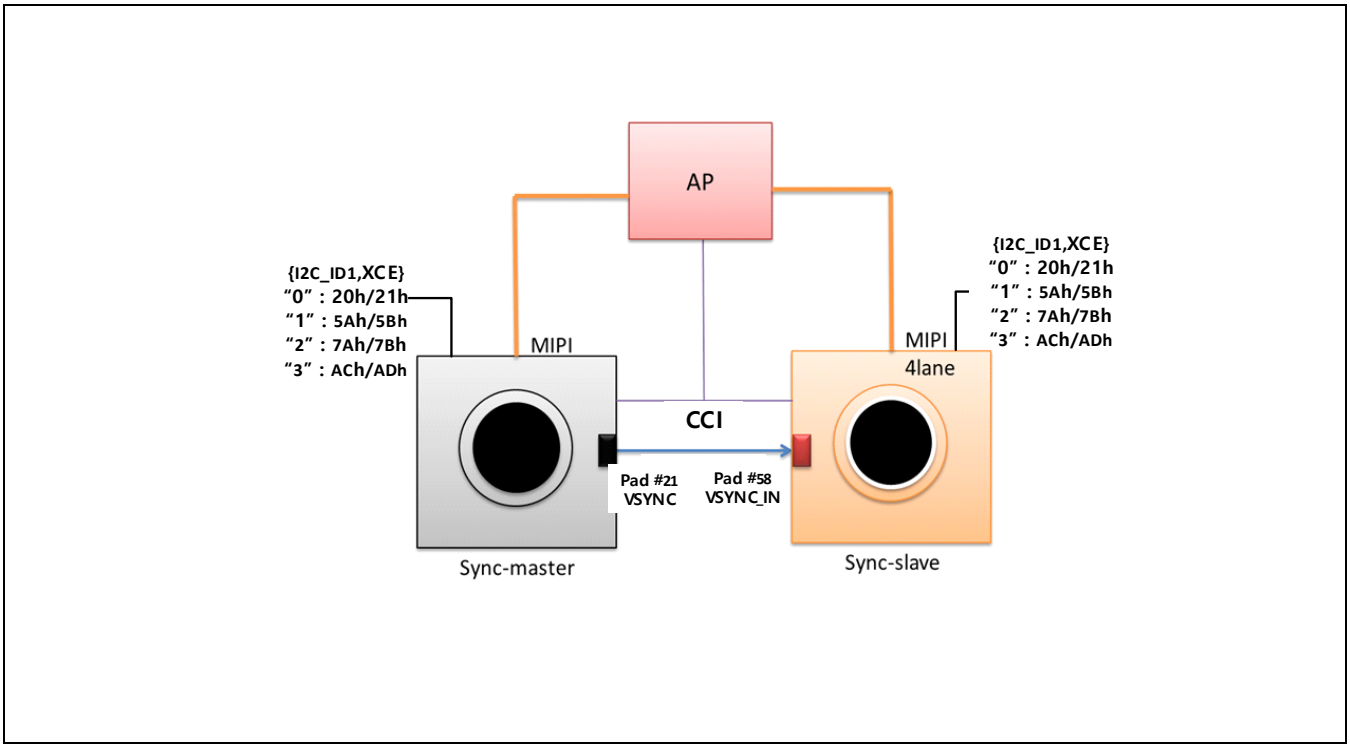

Figure 28 Dual sensor sync system

5.11 Test Pattern

S5KJNSSQ33 is configured to generate deterministic test patterns. For more information, refer to S5KJNSSQ33 Application Notes.

5.12 Output Data Interface

S5KJNSSQ33 MIPI CSI-2 interface is a four-lane high-speed serial interface that connects the camera sensor to a host processor. Maximum bitrate of MIPI of S5KJNSSQ33 is 2.15 Gbps per lane.

S5KJNSSQ33 supports all mandatory requirements in MIPI CSI-2 version 1.00 and DPHY 1.2 specifications. For more information, refer to MIPI DPHY 1.2 Specification.

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Table 20 Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit
Digital	VDDD (Max.)	–0.5	–	1.5	V
Analog 2.8	VDDA28 (Max.)	–0.3	–	3.6	
I/O	VDDIO (Max.)	–0.5	–	2.5	
Digital input voltages (1)	VIP (Max.)	–0.3	–	VDDIO + 0.3	
VCAP analog voltage (2)	VCAP	-0.3	–	4.2	
Storage temperature	TSTR	–40	–	85	°C

NOTE:

1. Digital Inputs: MCLK, RSTN, TST, I2C_SPI_N_SEL, XCE, SDO, SDI, SCK and GPIO_1/2/3, I2C_ID1, VSYNC_VSYNC_IN, HSYNC
2. Voltage on external capacitor onnected to analog output (VCAP refers to capacitor connected to analog power supplies such as VNTG, VRG, VSEL, VTG)

6.2 Operating Conditions

Table 21 Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
Digital power supply (1)	VDDD	0.95	1.05	1.15	V
Analog power supply (2)	VDDA28	2.7	2.8	2.9	
I/O supply	VDDIO	1.7	1.8	1.9	
Digital input voltages (3)	VIP	0	–	VDDIO	
VCAP analog voltage	VCAP	0	–	4.2	
Test temperature(T_a) (4)	TTEST	21	23	25	°C
Optimum operating temperature(T_j) (5)	TOPT	0	–	60	
Normal operating temperature(T_j) (6)	TOPR	–20	–	60	
Functional operating temperature(T_j) (7)	TFUNC	–20	–	85	

NOTE:

1. Digital supply tolerances
   Lower limit: 1.05 V – 100 mV
   Upper limit: 1.05 V + 100 mV
2. Analog supply tolerances
   Lower limit: 2.8 V – 100 mV
   Upper limit: 2.8 V + 100 mV
3. Digital inputs: MCLK, RSTN (XSHUTDOWN), TST, I2C_SPI_N_SEL, XCE, SDO, SDI, SCK, and GPIO_1/2/3, I2C_ID1, VSYNC_VSYNC_IN, HSYNC
4. Image quality test conditions
5. No visible degradation in image quality
6. Camera produces acceptable images
7. Camera fully functional

** All input power is the standard voltage of the chip input power pad

6.3 DC Characteristics

Table 22 DC Characteristics

(VDDA = 2.7 V to 2.9 V, VIP = 1.8 V ± 0.1 V, T_j = – 20 to + 85 °C, CLOAD = 20 pF)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	VIH	–	0.7 × VIP	–	VIP + 0.3	V
	VIL	–	–0.3	–	0.3 × VIP	
Input leakage current	IIL	VIN = VIP or VSS	–10	–	10	µA
High level output voltage	VOH	IOH = –100µA	VDDIO – 0.2	–	–	V
Low level output voltage	VOL	IOL = 100µA	–	–	0.2	
High-Z output leakage current	IOZ	VOUT = VSS or VDDD	– 10	–	10	µA
Input capacitance	CIN	–	–	–	5	pF
Supply current	IHWSBA (1)	Hardware standby mode analog	–	833.33	1000.00	µA
	IHWSBD (1)	Hardware standby mode digital	–	1.54	2.00	mA
	IHWSBIO (1)	Hardware standby mode IO	–	400.00	500.00	µA
	ISWSBA (2)	Software standby mode analog	–	833.33	1000.00	µA
	ISWSBD (2)	Software standby mode digital	–	38.46	50.00	mA
	ISWSBIO (2)	Software standby mode IO	–	400.00	500.00	µA
	ISTSUMA (2)	Streaming mode analog 12.5M@30fps (summation mode)	–	49.20	59.04	
	ISTSUMD (2)	Streaming mode digital 12.5M@30fps (summation mode)	–	167.00	217.10	
	ISTSUMIO (2)	Streaming mode digital IO 12.5M@30fps (summation mode)	–	2.00	4.00	

NOTE:

1. IHWSBA (analog), IHWSBD (digital) - RSTN assertion is needed.
2. Conditions: VDDA = 2.8 V, VDDD = 1.05 V, VDDIO = 1.8 V, T_j = 60 °C

6.4 AC Characteristics

Table 23 AC Characteristics

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock frequency (1)	fXCLK	–	12.0	–	64.0	MHz
External clock duty cycle	fXDUTY	–	45	–	55	%
PLL locking time	tLOCK	–	--	–	500	µs

NOTE: Applied to MCLK pin

1. External clock exceeding 14MHz is needed to operate fast-mode I2C bus device and external clock exceeding 16MHz is needed to operate fast-mode plus I2C-bus device.

7 Lens Specification

7.1 Target CRA (Chief Ray Angle)

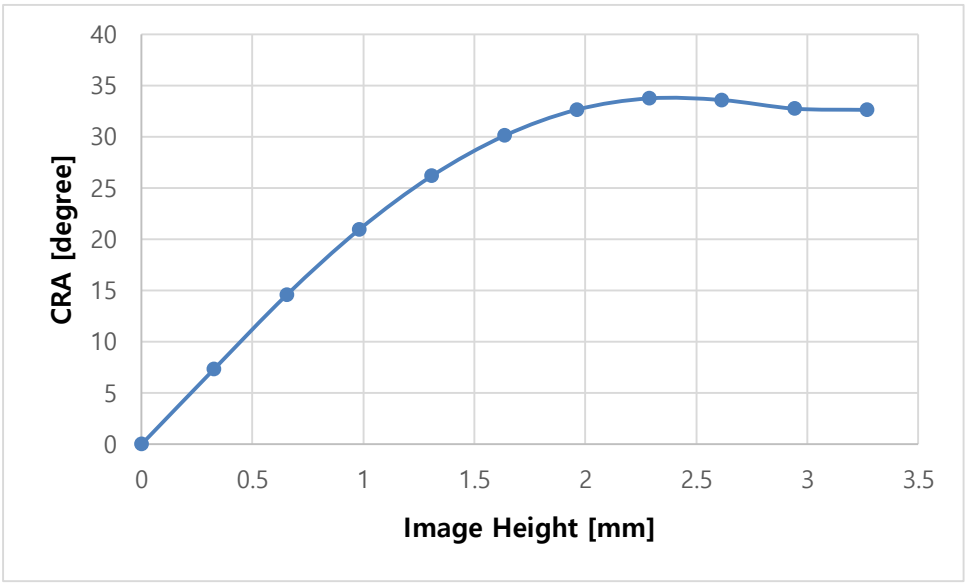

Table 24 Image Height (Field)

Image Height	mm	CRA (deg)
0	0	0
0.1	0.327	7.34
0.2	0.654	14.57
0.3	0.981	20.95
0.4	1.308	26.18
0.5	1.635	30.1
0.6	1.961	32.64
0.7	2.288	33.75
0.8	2.615	33.59
0.9	2.942	32.75
1	3.269	32.63

7.2 Pixel-Shading characteristics

Figure 29 illustrates shading characteristics of green pixel over difference between CRA and target CRA of given lens.

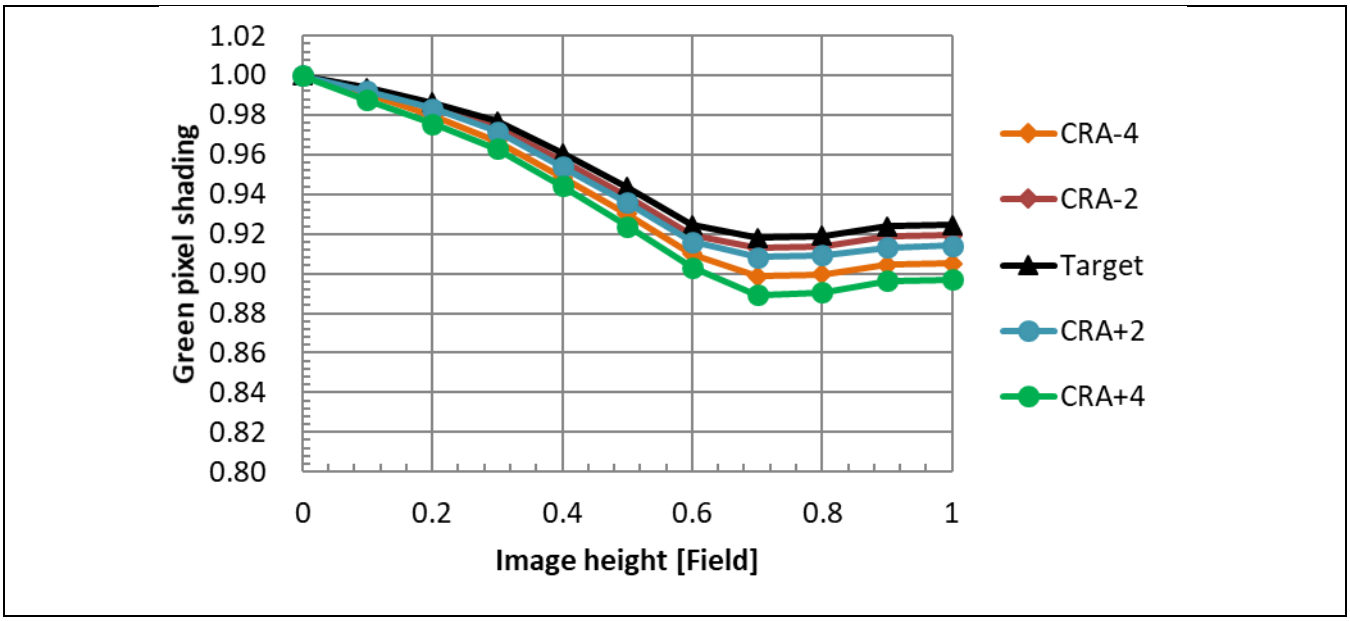

Figure 29 Shading Characteristics of Green

Figure 30 illustrates color ratio of B/G and R/G over the target CRA by image height.

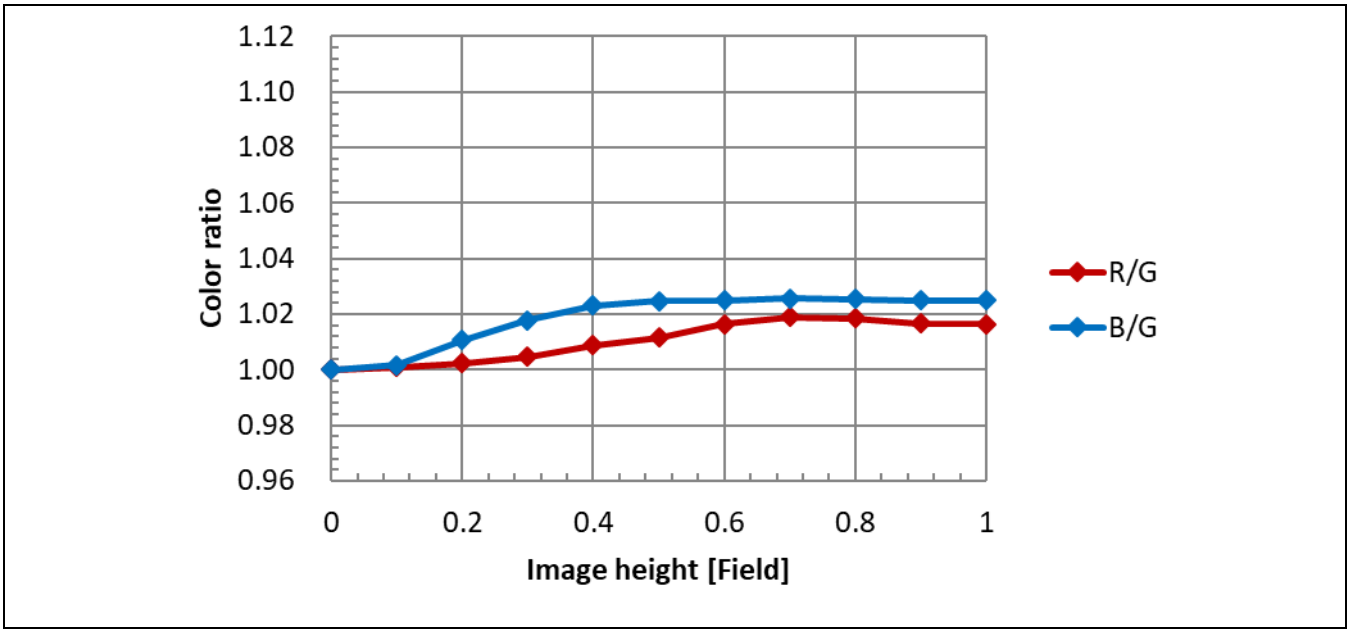

Figure 30 Shading Characteristics of Color ratio

7.3 Spectral Response

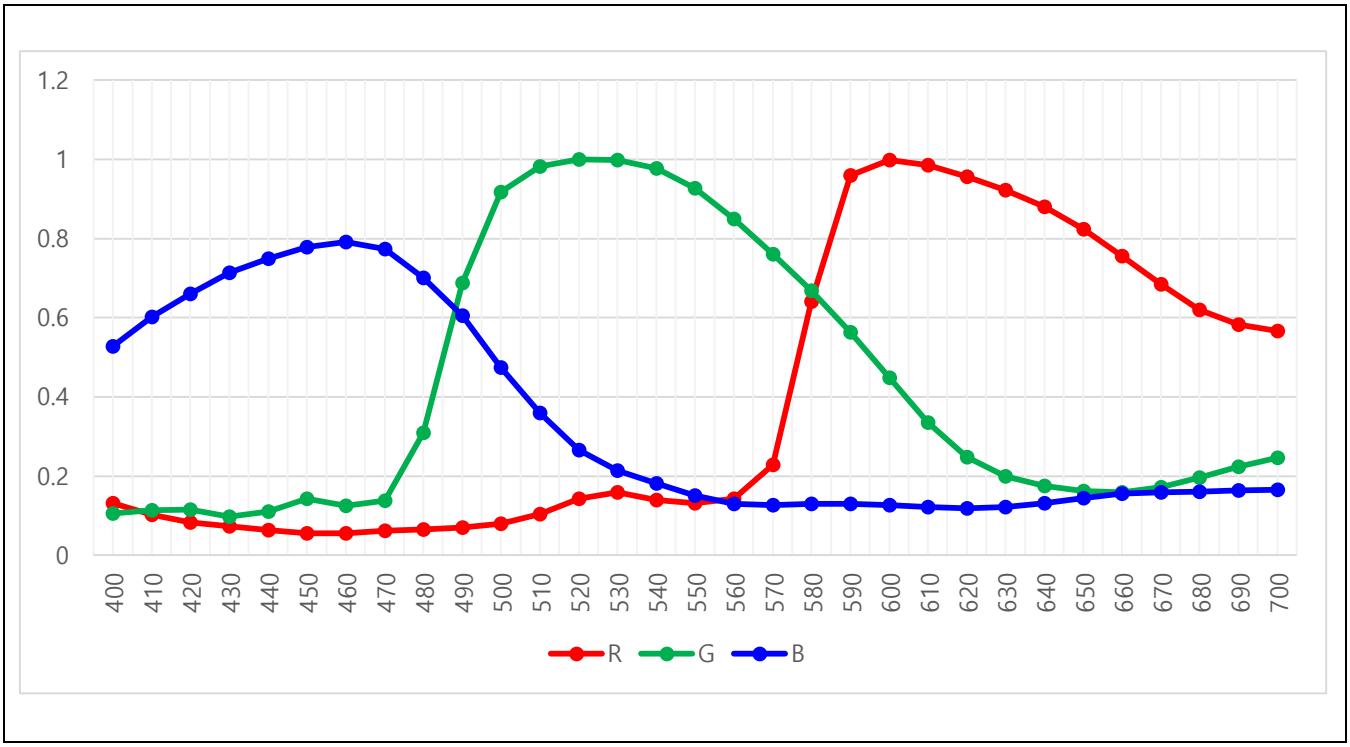

Figure 31 Spectral Response

Table 25 Spectral Response

Wavelength (nm)	R	G	B	Wavelength (nm)	R	G	B
400	0.132	0.105	0.527	550	0.132	0.927	0.151
410	0.102	0.114	0.602	560	0.142	0.849	0.13
420	0.082	0.115	0.661	570	0.229	0.761	0.126
430	0.073	0.098	0.714	580	0.641	0.668	0.13
440	0.063	0.11	0.75	590	0.959	0.564	0.13
450	0.056	0.142	0.778	600	0.999	0.449	0.127
460	0.055	0.125	0.791	610	0.986	0.335	0.122
470	0.061	0.137	0.773	620	0.957	0.248	0.118
480	0.065	0.309	0.7	630	0.923	0.2	0.121
490	0.069	0.688	0.605	640	0.88	0.175	0.131
500	0.08	0.918	0.475	650	0.824	0.162	0.145
510	0.104	0.983	0.36	660	0.756	0.159	0.155
520	0.143	1	0.265	670	0.684	0.171	0.159
530	0.158	0.999	0.213	680	0.62	0.196	0.16
540	0.14	0.978	0.182	690	0.582	0.223	0.164
				700	0.567	0.246	0.166

7.4 IR-cut filter selection

Figure 32 illustrates IR response of blue channel. Performance of IR-cut filter is very important for image quality at low color temperature. Samsung recommends IR cut filter with cut off from 650 nm to 1200 nm.

Figure 32 IR Response of Blue channel

8 Register Description

This chapter describes the register map information and its associated registers of S5KJNSSQ33.

Vendor registers are defined for extended functionality control.

8.1 Configuration Register

Table 26 Configuration Register

Name	Address	Size	Reset Value	Access Type	Description
api_rd_general_model_id	0x40000000	0x0002	0x38EF	RO	Camera module model identification number.
api_rd_general_revision_number_major	0x40000002	0x0001	0xA0	RO	Revision identifier of camera module for tuning/settings change.
api_rd_general_manufacturer_id	0x40000003	0x0001	0x00	RO	Module manufacturers code.
api_rd_general_api_version	0x40000004	0x0001	0x50	RO	API version.
api_rd_general_frame_count	0x40000005	0x0001	0x00	RO	0 = Wakeup (before first frame). 0xFF = SW stand by.

Name	Address	Size	Reset Value	Access Type	Description
					1-254 = Frame counter value.
api_rd_general_pixel_order	0x40000006	0x0001	0x00	RO	Color pixel order
api_rd_general_config_count	0x40000007	0x0001	0x00	RO	Configuration change counter(frames aborted or corrupted frames).
api_rd_general_data_pedestal	0x40000008	0x0002	0x0040	RO	Data pedestal - typically code 64 for 10-bit systems
api_rd_general_frame_id	0x4000000A	0x0001	0x00	RO	used for Auto Exposure Bracketing to set a value for AEB frames
api_rd_general_pixel_depth	0x4000000C	0x0001	0x0A	RO	8-bit, 10-bit or 12-bit pixel data
api_rd_general_color_filter_pattern	0x4000000D	0x0001	0x50	RO	Color filter pattern: 0x00 - Bayer GRBG without pdaf

Name	Address	Size	Reset Value	Access Type	Description
					0x10 - Bayer GRBG with pdaf 0x20 - RBW without pdaf 0x30 - RBW with pdaf 0x40 - Black and while CF (all active pixels has the same CF) without pdaf 0x50 - Tetracell pattern (2x2 Quadra CF) without PDAF 0x60 - Tetracell pattern (2x2 Quadra CF) with super PDAF

Name	Address	Size	Reset Value	Access Type	Description
					0x70 - Tetracell pattern (2x2 Quadra CF) with normal PDAF 0x80 - Black and while CF (all active pixels has the same CF) with PDAF 0x90 - Chessboard pattern 1/2 pixel are Iris and 1/2 are Depth
api_rd_general_cra	0x4000000E	0x0001	0x00	RO	CRA - Chief Ray Angle.
api_rd_general_sample_type	0x4000000F	0x0001	0x01	RO	0x01 = Typical sample. 0x00 = Random, Corner samples.
api_rd_general_revision_number_minor	0x40000010	0x0001	0x00	RO	Device revision identifier of the camera module for minor changes.

Name	Address	Size	Reset Value	Access Type	Description
api_rd_general_additional_specification_version	0x40000011	0x0001	0x06	RO	Internal version for customer use
api_rd_general_module_date_year	0x40000012	0x0001	0x00	RO	Bits[3:0] - Last digit of manufacturing year.
api_rd_general_module_date_month	0x40000013	0x0001	0x00	RO	Bits[3:0] - Manufacturing month.
api_rd_general_module_date_day	0x40000014	0x0001	0x00	RO	Bits[3:0] - Manufacturing day.
api_rd_general_module_date_phase	0x40000015	0x0001	0x01	RO	Bits[2:0] - Manufacturing phase.
api_rd_general_sensor_model_id	0x40000016	0x0002	0x0000	RO	Silicon identification number
api_rd_general_sensor_revision_number	0x40000018	0x0001	0x00	RO	Device Revision Identifier of sensor silicon.
api_rd_general_sensor_manufacturer_id	0x40000019	0x0001	0x00	RO	Manufacturers Code. Please refer the GIIC Manufacturer Codes Document.

Name	Address	Size	Reset Value	Access Type	Description
api_rd_general_sensor_firmware_version	0x40000001A	0x0002	0x0000	RO	Sensor firmware version.
api_rd_general_serial_number	0x40000001C	0x0002	0x0000	RO	Running serial number.
api_rd_general_sensor_setfile_version	0x40000001E	0x0002	0x0000	RO	Running setfile version number.
api_rd_general_temperature	0x40000020	0x0002	0x0000	RO	Temperature in Degrees (Celsius). Signed number with 8 fraction bits
api_rd_frame_format_model_type	0x40000040	0x0001	0x04	RO	1 = 2 bytes data format.
api_rd_frame_format_model_subtype	0x40000041	0x0001	0x11	RO	Bits[7:4] - number of horizontal descriptors. Bits[3:0] - number of vertical descriptors.
api_rd_frame_format_descriptor_0	0x40000042	0x0002	0x5000	RO	Bits [15:12] - Descriptor type.

Name	Address	Size	Reset Value	Access Type	Description
					Bits [11:0] - Descriptor Size
api_rd_frame_format_descriptor_1	0x40000044	0x0002	0x5820	RO	Bits [15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_2	0x40000046	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_3	0x40000048	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_4	0x4000004A	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size

Name	Address	Size	Reset Value	Access Type	Description
api_rd_frame_format_descriptor_5	0x4000004C	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_6	0x4000004E	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_7	0x40000050	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_8	0x40000052	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_9	0x40000054	0x0002	0x0000	RO	Bits[15:12] - Descriptor type.

Name	Address	Size	Reset Value	Access Type	Description
					Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_10	0x40000056	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_11	0x40000058	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_12	0x4000005A	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_13	0x4000005C	0x0002	0x0000	RO	Bits[15:12] - Descriptor type.

Name	Address	Size	Reset Value	Access Type	Description
					Bits[11:0] - Descriptor Size
api_rd_frame_format_descriptor_14	0x40000005E	0x0002	0x0000	RO	Bits[15:12] - Descriptor type. Bits[11:0] - Descriptor Size
api_rd_analog_gain_analog_gain_capability	0x40000080	0x0002	0x0002	RO	Describes the sensor analog gain capabilities. 0=Single global analog gain only 1=Separate channel analog gains only 2=Analog gain per exposure Short/Long
api_rd_analog_gain_code_min	0x40000084	0x0002	0x0020	RO	Minimum recommended analog gain code

Name	Address	Size	Reset Value	Access Type	Description
api_rd_analog_gain_code_max	0x40000086	0x0002	0x0200	RO	Maximum recommended analog gain code
api_rd_analog_gain_code_step	0x40000088	0x0002	0x0001	RO	Analog gain code step size
api_rd_analog_gain_type	0x4000008A	0x0002	0x0000	RO	Analog gain coding type.
api_rd_analog_gain_m0	0x4000008C	0x0002	0x0001	RO	Analog gain m0 constant (16-bit signed integer)
api_rd_analog_gain_c0	0x4000008E	0x0002	0x0000	RO	Analog gain c0 constant (16-bit signed integer)
api_rd_analog_gain_m1	0x40000090	0x0002	0x0000	RO	Analog gain m1 constant (16-bit signed integer)
api_rd_analog_gain_c1	0x40000092	0x0002	0x0020	RO	Analog gain c1 constant (16-bit signed integer)
api_rd_data_format_model_type	0x400000C0	0x0001	0x01	RO	Data Format (0x01 = 2 Byte Data Format)

Name	Address	Size	Reset Value	Access Type	Description
api_rd_data_format_model_subtype	0x400000C1	0x0001	0x03	RO	Contains the number of data format descriptors used
api_rd_data_format_descriptor_0	0x400000C2	0x0002	0x0A0A	RO	Top 10-bits of internal pixel data. Transmitted as RAW10.
api_rd_data_format_descriptor_1	0x400000C4	0x0002	0x0A08	RO	Top 10-bits of internal pixel data compressed to 8-bits.Transmitted as RAW8.
api_rd_data_format_descriptor_2	0x400000C6	0x0002	0x0808	RO	Top 8-bits of internal pixel data. Transmitted as RAW8.
api_rd_data_format_descriptor_3	0x400000C8	0x0002	0x0000	RO	Data type descriptor - not used.
api_rd_data_format_descriptor_4	0x400000CA	0x0002	0x0000	RO	Data type descriptor - not used.
api_rd_data_format_descriptor_5	0x400000CC	0x0002	0x0000	RO	Data type descriptor - not used.

Name	Address	Size	Reset Value	Access Type	Description
api_rd_data_format_descriptor_6	0x400000CE	0x0002	0x0000	RO	Data type descriptor - not used.
api_rd_current_state_tg_clk_khz	0x400000D0	0x0004	0x00000000	RW	Logical TGCLK (on ASIC it's always same as system clock) .
api_rd_current_state_pixel_clk_khz	0x400000D4	0x0004	0x00000000	RW	the ISP clk * the number of pixels processed in each clk.
api_rd_current_state_mipi_clk_khz	0x400000D8	0x0004	0x00000000	RW	the MIPI clk.
api_rd_current_state_vendor_error_type	0x400000DC	0x0002	0x0000	RW	System level error, caused by wrong user configuration: 0 - No error. 1 - External clock is not defined. 2 - External clock is defined, but out of range.

Name	Address	Size	Reset Value	Access Type	Description
					10 - Main pll pre_pll_clk_div is out of range. 11 - Main pll pll_ip_freq is out of range. 12 - Main pll pll_multiplier is out of range. 13 - Main pll pll_s divider is out of range. 14 - Main pll VCO freq is out of range.

Name	Address	Size	Reset Value	Access Type	Description
					15 - Main pll FOUT freq is out of range. 20 - Mipi pll pre_pll_clk_div is out of range. 21 - Mipi pll pll_ip_freq is out of range. 22 - Mipi pll pll_multiplier is out of range. 23 - Mipi pll pll_s divider is out of range. 24 - Mipi pll VCO freq is out of range. 25 - Mipi pll FOUT freq is out of range. 30 - vt_sys_div is out of range. 31 - vt_pix_div is out of range. 32 - vt_sys_freq is out of range.

Name	Address	Size	Reset Value	Access Type	Description
					33 - vt_pix_freq is out of range. 34 - op_sys_div is out of range. 35 - op_pix_div is out of range. 36 - op_sys_freq is out of range . 37 - op_pix_freq is out of range. 38 - Ddr divider is out of range. 39 - DPHY freq divider is out of range. 50 - WDR is not allowed on configured binning mode. 60 - Two or more functions are assigned to same GPIO.

Name	Address	Size	Reset Value	Access Type	Description
					62 - Read from invalid OTP address. VENDOR_ERR_NOT_SUPPORTED_COLUMNS_SUBSAMPLING - Configured columns sub-sampling is not supported.
api_rd_current_state_fw_first_error	0x400000DE	0x0002	0x0000	RW	FW error - First FW error .
api_rd_current_state_fw_first_error_info	0x400000E0	0x0002	0x0000	RW	FW error - FW error information.
api_rd_current_state_isp1_output_width	0x400000E2	0x0002	0x0000	RW	Video output image width include margins.
api_rd_current_state_isp1_output_height	0x400000E4	0x0002	0x0000	RW	Video output image height include margins.

Name	Address	Size	Reset Value	Access Type	Description
api_rd_current_state_isp2_output_width	0x400000E6	0x0002	0x0000	RW	Virtual channel #2 output image width include margin.
api_rd_current_state_isp2_output_height	0x400000E8	0x0002	0x0000	RW	Virtual channel #2 output image height include margins.
api_rd_current_state_dual_sensor_sync_master_slave_status	0x400000EA	0x0001	0x00	RW	Master/slave status (read only) Bit [0] 1 = Slave mode is enabled. Bit [4] 1 = Master mode is enabled. (That is, 0x10)
api_rd_current_state_context_switching_current	0x400000EC	0x0001	0x00	RO	Selected Context. 0=Context A 1=Context B.
api_rd_current_state_context_switching_count	0x400000ED	0x0001	0x00	RO	Frame counter for new context.

Name	Address	Size	Reset Value	Access Type	Description
api_rd_current_state_gph_by_gpio_status	0x400000EE	0x0001	0x00	RO	
api_rd_current_state_fast_change_mode_mode_index	0x400000FA	0x0001	0x00	RO	fast change mode only. current mode index.
api_rd_current_state_fast_change_mode_frame_down_counter	0x400000FB	0x0001	0x00	RO	fast change mode only. current frame count.
api_rd_current_state_fast_change_mode_loop_down_counter	0x400000FC	0x0001	0x00	RO	fast change mode only. current loop count.
api_rd_current_state_fast_change_mode_reference_pck	0x400000FE	0x0002	0x0000	RO	fast change mode only. reference pck.
api_rw_general_setup_mode_select	0x40000100	0x0001	0x00	RW/S	0 = Software Standby. 1 = Streaming.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_general_setup_image_orientation	0x40000101	0x0001	0x00	RW/C	Image orientation i.e. horizontal mirror and vertical flip. 0 = No horizontal mirror, no vertical flip. 1 = Horizontal mirror, no vertical flip. 2 = No horizontal mirror, vertical flip. 3 = Horizontal mirror and vertical flip.
api_rw_general_setup_software_reset	0x40000103	0x0001	0x00	RW/R	1 = Software reset.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_general_setup_grouped_parameter_hold	0x40000104	0x0001	0x00	RW/C	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters. 0 = Consume as normal, 1 = Hold.
api_rw_general_setup_mask_corrupted_frames	0x40000105	0x0001	0x01	RW	On Preserve timing mode 0 = Output the corrupted frame. 1 = Don't output the corrupted frame.
api_rw_general_setup_fast_standby_ctrl	0x40000106	0x0001	0x00	RW	0 = Frame completes before mode entry.

Name	Address	Size	Reset Value	Access Type	Description
					1 = Frame may be truncated before mode entry.
api_rw_general_setup_cci_address_control	0x40000107	0x0001	0x20	RW	Control CCI address. Expressed as 8 bit (e.g. 0x20 write, 0x21 read is entered as 0x20).
api_rw_general_setup_context_switching_select	0x40000108	0x0001	0x00	RW	Select Context. 0=Context A 1=Context B.
api_rw_general_setup_context_switching_frame_duration	0x40000109	0x0001	0x00	RW	Number of frames for Context switching
api_rw_general_setup_context_switc	0x4000	0x0	0x01		Context Mode:

Name	Address	Size	Reset Value	Access Type	Description
hing_mode	010A	001		RW	0=The user writes (and reads) Context A & Context B to the same virtual address. 1=The user writes (and reads) Context A & Context B to different virtual addresses.
api_rw_general_setup_immediate_exposure_enable	0x40000010F	0x0001	0x00	RW	start exposure of next frame immediately (in case exposure hasn't start yet). 0 = Disable immediate update for integration time and analog gain.

Name	Address	Size	Reset Value	Access Type	Description
					1 = Enable immediate update for integration time and analog gain.
api_rw_output_channel_identifier	0x40000110	0x0001	0x10	RW	Virtual channel number. [1:0] = VC of isp1 - Main video channel.
api_rw_output_signalling_mode	0x40000111	0x0001	0x02	RW	0 = PVI. 2 = CSI-2 with DPHY (MIPI)
api_rw_output_data_format	0x40000112	0x0002	0x0A0A	RW/C	Data Format: [15:8] = Max Sensors ADC resolution. [7:0] = output data format:

Name	Address	Size	Reset Value	Access Type	Description
					0x08: Top 8 bit of pixel data (RAW8). 0x0A Top 10 bits of pixel data (RAW10).
api_rw_output_lane_mode	0x40000114	0x0001	0x03	RW	Number of CSI-2 lanes to be used. 0 = 1 lane. 1= 2 lanes. 2 = 3 lanes. 3 = 4 lanes.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_output_isp2_output_mode	0x40000115	0x0001	0x00	RW	ISP2 (second stream) stream output mode. please note that the block that generates the stream must be enabled too. select which data to output by the ISP2 API_ISP2_OUTPUT_DISABLE - 0 - disable ISP2. API_ISP2_OUTPUT_PDAF - 1 - output PDAF stream.
api_rw_output_isp2_data_type	0x40000116	0x0001	0x30	RW	Isp2 Data type.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_output_embedded_as_active_enable	0x40000117	0x0001	0x00	RW	for debug footer, use this to allow the embedded to be output as (active) video lines.
api_rw_output_emb_use_header	0x40000118	0x0001	0x00	RW	0 = Disable heading embedded line 1 = Enable heading embedded line
api_rw_output_emb_header_lines	0x40000119	0x0001	0x02	RW	Defines the number of embedded lines (1-4).
api_rw_output_emb_footer_lines	0x4000011A	0x0001	0x00	RW	0 = Disable footering embedded line. 1 = Enable footering embedded line
api_rw_output_emb_equal_to_data	0x4000011B	0x0001	0x01	RW	Keep embedded line same length as pixels line:

Name	Address	Size	Reset Value	Access Type	Description
					0 = Embedded line length is shorter then data line length 1 = Embedded line length is equal to data line length. Note:this is only the line length, not the actual byte that used for data (fixed to 256 pixels each line).
api_rw_output_emb_in_bytes	0x4000011C	0x0001	0x01	RW	Keep embedded line pixel bitage same as pixels data bitage. 1 = Each embedded line pixel is byte

Name	Address	Size	Reset Value	Access Type	Description
					0 = Each embedded line pixel is equal to data pixel.
api_rw_output_qual_mode_continues_enable	0x4000011E	0x0001	0x01	RW	0 = Use qual mode options 1 = Use legacy mode of continuous clock (PVI clock always on)
api_rw_output_standby_power_mode	0x4000011F	0x0001	0x00	RW	MIPI DPHY standby power mode: 0 = ULPM. 1 = LP11 - lane lines stays high. 2 = Disabled (lane lines disconnected)
api_rw_op_cond_vana_voltage	0x40000130	0x0002	0x0028		Not in use.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_op_cond_vdig_voltage	0x40000132	0x0002	0x0012		Not in use.
api_rw_op_cond_vio_voltage	0x40000134	0x0002	0x0018		Not in use.
api_rw_op_cond_extclk_frequency_mhz	0x40000136	0x0002	0x1800	RW/S	Nominal External clock frequency (8.8 fixed point number).

Name	Address	Size	Reset Value	Access Type	Description
api_rw_op_cond_extclk_scale_up	0x40000013D	0x0001	0x00	RW	Allows using input clock higher than 255.99MHz. For example, input clock 260MHz will be set as 0x8200 on op_cond_extclk_frequency_mhz, and as 0x01 on this vendor register (130MHz << 1 = 260MHz). For example, input clock 260MHz will be set as 0x8200 (130MHz) on api register api_rw_op_cond_extclk_frequency_mhz, and as 0x01 on this vendor register (130MHz << 1 = 260MHz).

Name	Address	Size	Reset Value	Access Type	Description
api_rw_op_cond_extclk_frequency_additional_fraction_khz	0x40000013E	0x0002	0x0000	RW/S	additional fraction of external frequency given in khz. external frequency is (extclk_frequency_mhz * 1000/256) << extclk_scale_up + extclk_frequency_additional_fraction_khz
api_rw_integration_time_fine_integration_time	0x40000200	0x0002	0x0100	RW	Fine integration time (of short exposure in WDR mode) in Pixel clocks.
api_rw_integration_time_coarse_integration_time	0x40000202	0x0002	0x0006	RW	Coarse integration time in h-times (of short exposure in WDR mode)

Name	Address	Size	Reset Value	Access Type	Description
api_rw_analog_gain_code_global	0x40000204	0x0002	0x0020	RW	Global analog gain code (on WDR: for short exposure pixels) (8.5 format) example: gain x1 = 32d, gain x1.5 = 48d gain x4 = 128d
api_rw_digital_gain_digital_to_analog_gain_control	0x4000020C	0x0001	0x00	RW	0 - do not change gain control. 1 - move as much gain from digital to analog gain, separate for long and short. for gain product above 16, the rest will be in digital gain.

Name	Address	Size	Reset Value	Access Type	Description
					2 - set both long and short analog gains to the minimum of the 2, and convert the rest to digital gain. NOTE: mode 1, 2 only work with api_rw_digital_gain_mode == 0 / 2. i.e. only 1 digital gain value for short and for long.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_digital_gain_digital_gain_mode	0x4000020D	0x0001	0x00	RW/F	Use digital gain mode: 0 - use one gain for all short channels taken from api_rw_digital_gain_gains_green_red, and one gain for all long channels taken from api_rw_wdr_ext_long_digital_gain_green_red. 1- gain for each channel (Not supported on WDR modes!). 2 - use a single digital gain for short and long digital gains, taken from api_rw_digital_gain_gains_green_red.
api_rw_digital_gain_gains_green_red	0x4000020E	0x0002	0x0100	RW	Green (Red Row) channel digital gain value.Gain x1 = digital_gain_step_size

Name	Address	Size	Reset Value	Access Type	Description
api_rw_digital_gain_gains_red	0x40000210	0x0002	0x0100	RW	Red channel digital gain valueGain x1 = digital_gain_step_size
api_rw_digital_gain_gains_blue	0x40000212	0x0002	0x0100	RW	Blue channel digital gain valueGain x1 = digital_gain_step_size
api_rw_digital_gain_gains_green_blue	0x40000214	0x0002	0x0100	RW	Green (Blue Row) channel digital gain valueGain x1 = digital_gain_step_size
api_rw_clocks_vt_pix_clk_div	0x40000300	0x0002	0x0006	RW/S	Video Timing Pixel Clock divider.
api_rw_clocks_vt_sys_clk_div	0x40000302	0x0002	0x0001	RW/S	Video Timing System Clock Divider Value
api_rw_clocks_vt_pre_pll_clk_div	0x40000304	0x0002	0x0004	RW/S	Pre PLL clock Divider Value

Name	Address	Size	Reset Value	Access Type	Description
api_rw_clocks_vt_pll_multiplier	0x40000306	0x0002	0x008C	RW/S	PLL multiplier Value
api_rw_clocks_op_pix_clk_div	0x40000308	0x0002	0x0008	RW/S	Output Pixel Clock Divider
api_rw_clocks_op_sys_clk_div	0x4000030A	0x0002	0x0001	RW/S	Output System Clock Divider Value
api_rw_clocks_vt_pll_post_scaler	0x4000030C	0x0002	0x0000	RW/C	2^S divider (PLL Freq = Fvco/2^s) divider.
api_rw_clocks_op_pre_pll_clk_div	0x4000030E	0x0002	0x0004	RW/S	mipi PLL Pre PLL clock Divider Value
api_rw_clocks_op_pll_multiplier	0x40000310	0x0002	0x00A7	RW/S	mipi PLL multiplier Value
api_rw_clocks_op_pll_post_scaler	0x40000312	0x0002	0x0000	RW/C	MIPI PLL 2^S divider.
api_rw_clocks_vt_pll_multiplier_fraction	0x40000320	0x0002	0x0000	RW/S	PLL multiplier fractional value
api_rw_clocks_op_pll_multiplier_fraction	0x40000322	0x0002	0x0000	RW/S	MIPI PLL multiplier fractional value

Name	Address	Size	Reset Value	Access Type	Description
api_rw_mipi_freq_hopping_enable	0x40000328	0x0001	0x00	RW	Enable the support for MIPI PLL frequency hopping (FH).
api_rw_mipi_freq_hopping_pll_m_shift_on	0x40000329	0x0001	0x00	RW	Request for MIPI PLL frequency hopping (FH). 0 = use 'default' MIPI PLL (M)ultiplier value. 1 = use shifted MIPI PLL (M)ultiplier value.
api_rw_frame_timing_dynamic_frame_rate_enable	0x40000335	0x0001	0x00	RW	Enable dynamic frame rate. frame rate change according to integration time, but not smaller than frame_length_lines

Name	Address	Size	Reset Value	Access Type	Description
api_rw_frame_timing_frame_length_lines	0x40000340	0x0002	0x1894	RW	Frame Length in timing lines. (Can be increase by "long_exposure" registers).
api_rw_frame_timing_line_length_pck	0x40000342	0x0002	0x1540	RW/C	Line length (H-time) in pixel clocks (VT clock domain) (Can be increase by "long_exposure" registers). (0 = FW select shortest time possible)
api_rw_image_size_x_addr_start	0x40000344	0x0002	0x0000	RW/C	X-address of the top left corner of the visible pixel data (offset from full image size).

Name	Address	Size	Reset Value	Access Type	Description
api_rw_image_size_y_addr_start	0x40000346	0x0002	0x0000	RW/C	Y-address of the top left corner of the visible pixel data (offset from full image size).
api_rw_image_size_x_addr_end	0x40000348	0x0002	0x1FFF	RW/C	X-address of the bottom right corner of the visible pixel data (offset from full image size).
api_rw_image_size_y_addr_end	0x4000034A	0x0002	0x181F	RW/C	Y-address of the bottom right corner of the visible pixel data (offset from full image size).
api_rw_image_size_x_output_size	0x4000034C	0x0002	0x2000	RW	Width of image data output from the sensor module.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_image_size_y_output_size	0x40000034E	0x0002	0x1820	RW	Height of image data output from the sensor module.
api_rw_image_size_digital_crop_x_offset	0x40000350	0x0002	0x0000	RW	Allow to cut off left side of output image (Crop&Pad)
api_rw_image_size_digital_crop_y_offset	0x40000352	0x0002	0x0000	RW	Allow to cut off top side of output image (Crop&Pad)
api_rw_sub_sample_x_even_inc	0x40000380	0x0002	0x0001	RW/C	Visible columns readout sub-sampling - even increment.
api_rw_sub_sample_x_odd_inc	0x40000382	0x0002	0x0001	RW/C	Visible columns readout sub-sampling - odd increment.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_sub_sample_y_even_inc	0x40000384	0x0002	0x0001	RW/C	Visible rows readout sub-sampling - even increment.
api_rw_sub_sample_y_odd_inc	0x40000386	0x0002	0x0001	RW/C	Visible rows readout sub-sampling - odd increment.
api_rw_scaling_cluster_digital_binning_factor	0x40000400	0x0002	0x0000	RW/C	tetracell Down scale factor: Range: 1 / 2 upwards Should determine only Bits[7:0] - Row (Vertical) scaling factor, 4 fraction bits. Bits[15:8] - Column (Horizontal) scaling factor, 4 fraction bits.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_scaling_hbin_digital_binning_factor	0x40000404	0x0001	0x00	RW/C	enable using digital horizontal binning NOTE: this digital binning is added onto the analog binning. 0 - do not use HBIN in digital. 0x10 - do not use HBIN in digital. 0x20 - use FE-ISP horizontal binning 2. and so on up to 0x80. also see t_isp_hbin... fields.
api_rw_scaling_digital_scaling_x	0x40000408	0x0002	0x0000		Column (horizontal) scaling factor (8 fraction bits)
api_rw_scaling_digital_scaling_y	0x4000040A	0x0002	0x0000		Row (vertical) scaling factor (8 fraction bits)

Name	Address	Size	Reset Value	Access Type	Description
api_rw_scaling_cluster_binning_mode	0x40000040C	0x0001	0x11	RW	Bits [2:0]: 1 = Enable digital cluster row (vertical) averaging. 2 = Enable digital cluster row (vertical) summation. 3 = Digital cluster pixel selection on HDR modes 4 = Enable digital cluster row. (vertical) median (Nona pattern only). 5 = Digital cluster row (vertical) split only Bits [6:4]:

Name	Address	Size	Reset Value	Access Type	Description
					1 = Enable digital cluster column (horizontal) averaging. 2 = Enable digital cluster column (horizontal) summation. 3 = Digital cluster pixel selection on HDR modes 4 = Enable digital cluster column (horizontal) median (Nona pattern only). 5 = Digital cluster column (horizontal) split only

Name	Address	Size	Reset Value	Access Type	Description
api_rw_compression_compression_mode	0x40000500	0x0002	0x0000	RW	0 = Compression disabled. 1 = Compression enabled.
api_rw_test_pattern_test_pattern_mode	0x40000600	0x0002	0x0000	RW	Controls the output of the test pattern module 0=no pattern (default) 1= solid colour. 2= 100% colour bars 3= fade to grey colour bars 4=PN9.
api_rw_test_pattern_test_data_green_red	0x40000602	0x0002	0x0000	RW	The test data used to replace green pixel data on rows that also have red pixels
api_rw_test_pattern_test_data_red	0x40000604	0x0002	0x0000	RW	The test data used to replace red pixel data.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_test_pattern_test_data_blue	0x40000606	0x0002	0x0000	RW	The test data used to replace blue pixel data
api_rw_test_pattern_test_data_green_blue	0x40000608	0x0002	0x0000	RW	The test data used to replace green pixel data on rows that also have blue pixels.
api_rw_test_pattern_horizontal_cursor_width	0x4000060A	0x0002	0x0000	RW	Defines the width of the horizontal cursor (in pixels)
api_rw_test_pattern_horizontal_cursor_position	0x4000060C	0x0002	0x0000	RW	Defines the top edge of the horizontal cursor
api_rw_test_pattern_vertical_cursor_width	0x4000060E	0x0002	0x0000	RW	Defines the width of the vertical cursor (in pixels)
api_rw_test_pattern_vertical_cursor_position	0x40000610	0x0002	0x0000	RW	Defines the left hand edge of the vertical cursor.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_test_pattern_crc	0x40000612	0x0001	0x00	RW	Enable CRC calculation. Every last line, the data will be replaced with the 2 Bytes of CRC output.
api_rw_test_pattern_fade_aux	0x40000613	0x0001	0x00	RW	Quantization level of right side of each bar.
api_rw_test_pattern_fade_factor	0x40000614	0x0001	0x00	RW	Smooth fade to gray gradient.
api_rw_test_pattern_fedtp_gradient_enable	0x40000615	0x0001	0x00	RW	bit 1: gradient enable Y. bit 0: gradient enable X.
api_rw_test_pattern_fedtp_gradient_invert	0x40000616	0x0001	0x00	RW	bit 1: Invert address Y. bit 0: Invert address X.
api_rw_test_pattern_fedtp_gradient_hor_shift	0x40000617	0x0001	0x00	RW	Scaling factor for X dependent gradient.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_test_pattern_fedtp_gradient_ver_shift	0x40000618	0x0001	0x00	RW	Scaling factor for Y dependent gradient.
api_rw_test_pattern_fedtp_address_noise	0x40000619	0x0001	0x00	RW	Enable horizontal address dependent 6bits noise.
api_rw_test_pattern_fedtp_hor_addr_noise_shift	0x4000061A	0x0001	0x00	RW	Right shift for Horizontal Noise generated values.
api_rw_test_pattern_fedtp_ver_addr_noise_shift	0x4000061B	0x0001	0x00	RW	Right shift for Vertical Noise generated values.
api_rw_test_pattern_fedtp_random_noise_right	0x4000061C	0x0001	0x00	RW	Right shift the random LFSR14 values.
api_rw_test_pattern_fedtp_mode56_shift_right	0x4000061D	0x0001	0x00	RW	Right shift for modes 5 and 6 generated values.
api_rw_long_frame_timing_frame_length_lines_sh	0x40000702	0x0001	0x00	RW/C	Left shifter for frame length in lines (max value is 11).

Name	Address	Size	Reset Value	Access Type	Description
api_rw_long_frame_timing_line_length_pck_sh	0x40000703	0x0001	0x00	RW/C	shift-up value for line length pck.
api_rw_long_frame_timing_coarse_integration_time_sh	0x40000704	0x0001	0x00	RW/C	Left shifter for coarse integration time (max value is 11) Max exposure shouldn't be more than 1200 seconds.
api_rw_phy_dphy_requested_link_rate	0x40000800	0x0004	0x00000000	RW	Target bitrate for CSI-2 transmission: with D-PHY, this is bitrate (Mbit/s) in 16 fraction bits.
api_rw_phy_dphy_ctrl	0x40000804	0x0001	0x00	RW	0 = Use automatic control. 1 = Use UI control. 2 = Use register control.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_phy_dphy_skew_calibration_min_freq_mhz	0x40000806	0x0002	0x05DC	RW	Minimal frequency for invocation of SKEW synchronization (Added by samsung).
api_rw_phy_dphy_skew_periodic_calibration_control	0x40000808	0x0001	0x00	RW	0 = do not send calibration sequence. 2 = send calibration sequence during frame blanking.
api_rw_phy_dphy_skew_periodic_calibration_interval	0x40000809	0x0001	0x00	RW	Output frame interval of period skew calibration. 0=no output.

Name	Address	Size	Reset Value	Access Type	Description
					1=output with all frames. otherwise, output once by X frames. (for example, number 2 means every second frame.
api_rw_phy_dphy_skew_init_calibration_control	0x40000080A	0x0001	0x01	RW	Value 0: do not send calibration sequence Value 1: send calibration sequence during start of streaming.
api_rw_phy_dphy_timing_tclk_post	0x40000080E	0x0001	0x00	RW	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_phy_dphy_timing_ths_prepare	0x40000080F	0x0001	0x00	RW	THS-PREPARE, is the time to drive LP-00 before starting the HS transmission on a Data Lane.
api_rw_phy_dphy_timing_ths_zero_min	0x40000810	0x0001	0x00	RW	THS-ZERO, MIN is the time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_phy_dphy_timing_ths_trail	0x40000811	0x0001	0x00	RW	THS-TRAIL is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.
api_rw_phy_dphy_timing_tclk_trail_min	0x40000812	0x0001	0x00	RW	Time to drive HS differential state after last payload clock bit of a HS transmission burst.
api_rw_phy_dphy_timing_tclk_prepare	0x40000813	0x0001	0x00	RW	Time to drive LP-00 to prepare for HS clock transmission.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_phy_dphy_timing_tclk_zero	0x40000814	0x0001	0x00	RW	Time for lead HS-0 drive period before starting Clock.
api_rw_phy_dphy_timing_tlpx	0x40000815	0x0001	0x00	RW	Length of any Low-Power state period.
api_rw_phy_dphy_timing_ths_exit	0x40000816	0x0001	0x00	RW	ths_exit timing.
api_rw_binning_mode	0x40000900	0x0001	0x11	RW/C	0 = Analog binning disabled. 1 = Analog binning enabled. 2 = Analog summation enabled, only in 2PD projects.
api_rw_binning_type	0x40000901	0x0001	0x11	RW/C	[3:0] - Row (Vertical) Binning factor.

Name	Address	Size	Reset Value	Access Type	Description
					[7:4] - Column (Horizontal) Binning factor. for analog summation set row binning factor to 2 (in 2PD project only).
api_rw_binning_weighting	0x40000902	0x0001	0x00	RW/C	0=averaged weighting. 1 = summed weighting. 2 = Bayer weighting 3 = module-specific weighting.
api_rw_binning_use_dark_lines_bin	0x40000904	0x0001	0x01	RW/C	Analog vertical binning for dark lines
api_rw_data_transfer_ctrl	0x40000A00	0x0001	0x00	RW	Bit 0: 1 = enable, 0 = disable. Bit 1:

Name	Address	Size	Reset Value	Access Type	Description
					1 = write enable, 0 = read enable. Bit 2: 1 = pending errors, read errors register.(See Protocol documentation)
api_rw_data_transfer_errors	0x40000A01	0x0001	0x00	RW	Error flags: Bit 0 : data corrupted error (failed to read from OTP) Bit 1 : error bit wasn't cleared before operation. Bit 2 : trying to write to bit that is already set in OTP

Name	Address	Size	Reset Value	Access Type	Description
					Bit 3: request set (ctrl bit 0 set) while processing request. Bit 4: wrong page number.
api_rw_data_transfer_page_select	0x40000A02	0x0002	0x0000	RW	Page each page is 64 bytes. Do not exceed OTP size!
api_rw_data_transfer_data_0_	0x40000A04	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_1_	0x40000A05	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_2_	0x40000A06	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_3_	0x40000A07	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_4_	0x40000A08	0x0001	0x00	RW	64 x 8-bit register for read or write accesses

Name	Address	Size	Reset Value	Access Type	Description
api_rw_data_transfer_data_5_	0x40000A09	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_6_	0x40000A0A	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_7_	0x40000A0B	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_8_	0x40000A0C	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_9_	0x40000A0D	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_10_	0x40000A0E	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_11_	0x40000A0F	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_12_	0x40000A10	0x0001	0x00	RW	64 x 8-bit register for read or write accesses

Name	Address	Size	Reset Value	Access Type	Description
api_rw_data_transfer_data_13_	0x40000A11	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_14_	0x40000A12	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_15_	0x40000A13	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_16_	0x40000A14	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_17_	0x40000A15	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_18_	0x40000A16	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_19_	0x40000A17	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_20_	0x40000A18	0x0001	0x00	RW	64 x 8-bit register for read or write accesses

Name	Address	Size	Reset Value	Access Type	Description
api_rw_data_transfer_data_21_	0x40000A19	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_22_	0x40000A1A	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_23_	0x40000A1B	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_24_	0x40000A1C	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_25_	0x40000A1D	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_26_	0x40000A1E	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_27_	0x40000A1F	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_28_	0x40000A20	0x0001	0x00	RW	64 x 8-bit register for read or write accesses

Name	Address	Size	Reset Value	Access Type	Description
api_rw_data_transfer_data_29_	0x40000A21	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_30_	0x40000A22	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_31_	0x40000A23	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_32_	0x40000A24	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_33_	0x40000A25	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_34_	0x40000A26	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_35_	0x40000A27	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_36_	0x40000A28	0x0001	0x00	RW	64 x 8-bit register for read or write accesses

Name	Address	Size	Reset Value	Access Type	Description
api_rw_data_transfer_data_37_	0x40000A29	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_38_	0x40000A2A	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_39_	0x40000A2B	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_40_	0x40000A2C	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_41_	0x40000A2D	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_42_	0x40000A2E	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_43_	0x40000A2F	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_44_	0x40000A30	0x0001	0x00	RW	64 x 8-bit register for read or write accesses

Name	Address	Size	Reset Value	Access Type	Description
api_rw_data_transfer_data_45_	0x40000A31	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_46_	0x40000A32	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_47_	0x40000A33	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_48_	0x40000A34	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_49_	0x40000A35	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_50_	0x40000A36	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_51_	0x40000A37	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_52_	0x40000A38	0x0001	0x00	RW	64 x 8-bit register for read or write accesses

Name	Address	Size	Reset Value	Access Type	Description
api_rw_data_transfer_data_53_	0x40000A39	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_54_	0x40000A3A	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_55_	0x40000A3B	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_56_	0x40000A3C	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_57_	0x40000A3D	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_58_	0x40000A3E	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_59_	0x40000A3F	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_60_	0x40000A40	0x0001	0x00	RW	64 x 8-bit register for read or write accesses

Name	Address	Size	Reset Value	Access Type	Description
api_rw_data_transfer_data_61_	0x40000A41	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_62_	0x40000A42	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_data_transfer_data_63_	0x40000A43	0x0001	0x00	RW	64 x 8-bit register for read or write accesses
api_rw_dual_sensor_sync_enable	0x40000A70	0x0002	0x0000	RW	0 = Disable dual sensor sync 1 = Enable dual sensor sync
api_rw_dual_sensor_sync_master_slave_mode_sel	0x40000A72	0x0002	0x0001	RW	Bits [0:3]: Slave mode 0x0 = Slave mode is disabled. 0x1 = Slave mode is enabled. 0x2 = Slave mode is enabled, but no resync.

Name	Address	Size	Reset Value	Access Type	Description
					Bits [8:15]: Master mode, relevant only when outputting VSYNC-OUT at a different rate than 1 for each frame 0x0 = Master mode is disabled. 0x1 = Master mode is enabled. VSYNC-OUT MIPI starts. 0x2 = Master mode is enabled. VSYNC-OUT short exposure starts. 0x3 = Master mode is enabled. VSYNC-OUT long exposure starts.

Name	Address	Size	Reset Value	Access Type	Description
					NOTE: To work both master mode and slave mode together, they must use different GPIOs. If master and slave use the same GPIO and master_slave_mode_sel = 0x0000, then GPIO outputs Hi-Z.
api_rw_dual_sensor_sync_prompt_sync	0x40000A74	0x0002	0x0001	RW	0 = Disable 1 = Sync master and slave promptly by reducing/increasing the frame length lines as much as needed.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_dual_sensor_sync_gradual_sync	0x40000A76	0x0002	0x0001	RW	0 = Sync promptly between master and slave by reducing/increasing the frame length lines as much as needed. 1 = Sync master and slave gradually over many frames by reducing/increasing the slave frame time until sync is achieved. NOTE: This is relevant only for resync on-the-fly.
api_rw_dual_sensor_sync_master_sync_delay_lines	0x40000A78	0x0004	0x00000001	RW	Delay for master sync signal

Name	Address	Size	Reset Value	Access Type	Description
api_rw_dual_sensor_sync_master_sync_width_lines	0x40000A7C	0x0002	0x0032	RW	Width for master sync signal (number of lines)
api_rw_dual_sensor_sync_master_mode_vsync_out_ratio	0x40000A7E	0x0002	0x0001		If dual_sensor_sync_mode = DUAL_SENSOR_SYNC_MODE_MASTER, then this is the ratio to transmit the VSYNC-OUT signals.
api_rw_dual_sensor_sync_vsync_in_to_vsync_out_time	0x40000A80	0x0002	0x0001	RW	Time which should pass between the VSync-in to VSync-out signals. This is used to calculate the drift. This is configured in timing lines.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_isp_bitreduct_qe_method	0x40000B02	0x0001	0x01	RW	Bit Reduction method of quantization error (QE) 0 - floor. 1 - round. 2 - Error diffusion.
api_rw_isp_black_level_correction_enable	0x40000B05	0x0001	0x01	RW	0 = Black level correction disabled. 1 = Black level correction enabled (enable fadlc)
api_rw_isp_mapped_couplet_correct_enable	0x40000B06	0x0001	0x01	RW	0 = Disabled static bad pixels correction. 1 = Enable static bad pixels correction.
api_rw_isp_dithering_before_gains_enable	0x40000B07	0x0001	0x01	RW	bypass the dithering before mixer gains.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_isp_dithering_after_gains_enable	0x40000B08	0x0001	0x00	RW	bypass the dithering after mixer gains.
api_rw_isp_dynamic_couplet_correct_enable	0x40000B09	0x0001	0x00	RW	0 = Disabled Dynamic correction. 1 = Enable Dynamic Correction
api_rw_isp_msm_offsets_enable	0x40000B0A	0x0001	0x01	RW	MSM Offsets enable disable flag.
api_rw_isp_msm_gains_enable	0x40000B0B	0x0001	0x01	RW	MSM Gains enable disable flag. disabling this flag will result in MSM Periodic Gains to be set to 1.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_isp_msm_channel_gains_enable	0x40000B0C	0x0001	0x01	RW	MSM channel Gains enable disable flag. disabling this flag will result in MSM Channel Gains to be set to 1.
api_rw_fast_change_mode_enable	0x40000B30	0x0001	0x00	RW	fast change mode enable.
api_rw_fast_change_mode_mode_index	0x40000B31	0x0001	0xFF	RW	fast change mode, mode index. [0 - 6]: select mode , 0xff- do not apply any mode.
api_rw_fast_change_mode_frames_delay_number	0x40000B32	0x0001	0x00	RW	number of frames delay from request till execute configuration change.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_fast_change_mode_frames_number_on_new_config	0x40000B33	0x0001	0x00	RW	number of frames to run new configuration before changing back to previous config.
api_rw_fast_change_mode_continues_mode_change_enable	0x40000B34	0x0001	0x00	RW	continues change mode enable. 0 - disable, 1 - enable. if enable all other modes are discard.
api_rw_fast_change_mode_restore_saved_api_on_prev_mode	0x40000B35	0x0001	0x00	RW	save and restore prev mode api when back to previous mode is enabled. 0 - disable, 1 - enable.
api_rw_fast_change_mode_use_referenced_pck	0x40000B36	0x0001	0x00	RW	use a referenced pck for translating user exposure and/or FLL request.

Name	Address	Size	Reset Value	Access Type	Description
					[0:0] - for exposure, 0 - disable, 1 - enable. [1:1] - for FLL, 0 - disable, 1 - enable. [2:2] - for strobe, 0 - disable, 1 - enable.
api_rw_sensor_out_pedestal	0x40000BC0	0x0002	0x0040	RW	Output pedestal.
api_rw_sensor_offset_x	0x40000BC2	0x0002	0x0000	RW/C	Offset from X-address of the top left corner of the visible pixel data after analog crop, bin and subsample (resizer)

Name	Address	Size	Reset Value	Access Type	Description
api_rw_sensor_offset_y	0x40000BC4	0x0002	0x0000	RW/C	Offset from Y-address of the top left corner of the visible pixel data after analog crop, bin and subsample (resizer)
api_rw_sensor_out_type	0x40000BC6	0x0001	0x00	RW	0 = Visible only. 1 = Visible + Dark. 2 = Visible + TMC. 3 = Visible + Dark + TMC.
api_rw_sensor_physical_pixel_order	0x40000BC7	0x0001	0x00	RW	Defines color of physical pixel 0, 0:0: Gr Rg / Bg Gb1: Rg Gr / Gb Bg2: Bg Gb / Gr Rg3: Gb Bg / Rg Gr

Name	Address	Size	Reset Value	Access Type	Description
api_rw_sensor_static_bpc_calc_mode	0x40000BC9	0x0001	0x02	RW	this field is used to select when the static BPC calculations are done. 0 - offline. can cause the first frame to be without the BPC correction. 1 - during fast frame. adds time to the fast frame, if the exposure is too short. 2 - as part of FW configuration change.
api_rw_sensor_b_abort_timing_on_ch_cfg	0x40000BCA	0x0001	0x01	RW	0 = Preserve timing (Keep frame rate)

Name	Address	Size	Reset Value	Access Type	Description
					1 = Abort timing if next frame is corrupted (On configuration change)
api_rw_sensor_abort_timing_method_on_rolling_sh	0x40000BCB	0x0001	0x01	RW	This register describe when to Abort when using rolling shutter: 0 = Abort timing Immediately, even during read out. 1 = Abort timing after read out ends. 2 = Abort timing on end of frame.
api_rw_sensor_abort_timing_on_sw_stby	0x40000BCC	0x0001	0x01	RW	This register describe when to Abort when entering software standby:

Name	Address	Size	Reset Value	Access Type	Description
					0 = Abort timing Immediately, even during read out. 1 = Abort timing after read out ends. 2 = Abort timing on end of frame.
api_rw_sensor_right_offset_x	0x40000BE0	0x0002	0x0000	RW/C	Offset from X-address of the bottom right corner of the visible pixel data after analog crop, bin and subsample (resizer)

Name	Address	Size	Reset Value	Access Type	Description
api_rw_sensor_bottom_offset_y	0x40000BE2	0x0002	0x0000	RW/C	Offset from Y-address of the bottom right corner of the visible pixel data after analog crop, bin and subsample (resizer)

Name	Address	Size	Reset Value	Access Type	Description
api_rw_pdaf_pdaf_exist	0x40000D00	0x0001	0x01	RW	PDAF readout (in case APS have PDAF it's possible only on binning modes. PDAF pixels wont be averaged with normal pixels. No special treatment on ISP chain, BPC, H-Bin. 1 = enable PDAF readout. Enable PDAF readout .
api_rw_pdaf_pdaf_correct	0x40000D01	0x0001	0x01	RW	Enable PDAF defect correction on for visible pixel area.
api_rw_pdaf_pdaf_collection_enable	0x40000D02	0x0001	0x00	RW	Enable PD collect (Tail mode) .

Name	Address	Size	Reset Value	Access Type	Description
api_rw_pdaf_virtual_channel	0x40000D03	0x0001	0x01	RW	Register to control PDAF virtual channel when PDAF uses interleaved readout mode.
api_rw_pdaf_interleaved_enable	0x40000D04	0x0001	0x01	RW	1 = output pdaf interleaved (Tail mode). 0 = interlaced (according to bit 2, 3 on control register)
api_rw_pdaf_collect_from	0x40000D05	0x0001	0x02	RW	PD collect output. 0 - before H-bin. 2 - After Bit reduct.

Name	Address	Size	Reset Value	Access Type	Description
api_rw_pdaf_out_width	0x40000D06	0x0002	0x0000	RW	total PDAF tail output width (with padding). If set to 0 FW calculate the minimal width needed for PDAF in output image the width might be rounded up by 4. Monitor: m_oif_vc2_output_width .
api_rw_pdaf_out_height	0x40000D08	0x0002	0x0000	RW	total PDAF tail output height. If set to 0 FW calculate the minimal height needed for PDAF in output image Monitor: m_oif_vc2_output_height .

Name	Address	Size	Reset Value	Access Type	Description
api_rw_color_temperature_colour_temperature	0x40000D80	0x0002	0x1388	RW	Scene color temperature in Kelvins
api_rw_color_temperature_absolute_gain_red	0x40000D82	0x0002	0x0100	RW	Calculated Gain for red channel, in 8 fraction bits (max = x16)
api_rw_color_temperature_absolute_gain_green	0x40000D84	0x0002	0x0100	RW	Calculated Gain for green channels, in 8 fraction bits (max = x16)
api_rw_color_temperature_absolute_gain_blue	0x40000D86	0x0002	0x0100	RW	Calculated Gain for blue channel, in 8 fraction bits (max = x16)

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_control	0x40000E00	0x0001	0x00	RW	0 = disabled 1...n = bracketing over n frames. Maximum value of n is bracketing_LUT_size. If n is smaller than bracketing_LUT_size then camera will use only those n values from the bracketing LUT. E.g. if bracketing_LUT_size is 5, host can use bracketing only for 3 frames by setting bracketing_LUT_control to value 3.
api_rw_bracketing_lut_mode	0x4000	0x0	0x00		Bit 0:

Name	Address	Size	Reset Value	Access Type	Description
	0E01	001		RW	0 = return to SW Standby after bracketing, 1 = continue in streaming after bracketing Bit 1: 0 = single bracketing, 1 = loop mode. Bit 2-7:reserved for future use.
api_rw_bracketing_lut_entry_control	0x40000E02	0x0001	0x00		Reserved for future use.
api_rw_bracketing_loop_mode_num_of_repetitions	0x40000E03	0x0001	0x00	RW	When using loop mode (lut_mode[1] = 1), this field specifies the number of times to repeat the loop.

Name	Address	Size	Reset Value	Access Type	Description
					0 = Repeat the loop indefinitely. 1 ~ 0xFF = Number of times to repeat the loop
api_rw_bracketing_selected_fields	0x40000E04	0x0002	0x0000	RW	Bit 0: 1 = coarse integration time LUT entry supported Bit 1: 1 = global analog gain LUT entry supported Bit 2. 1 = coarse integration time LUT entry supported (long exposure) Bit 3:

Name	Address	Size	Reset Value	Access Type	Description
					1 = long exposure, global analog gain. Bit 4: 1 = flash LUT entry supported Bit 5: 1 = global digital gain LUT entry supported Bit 6-7: reserved for future use All bits: 0 = select all.
api_rw_bracketing_lut_0_	0x40000E10	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_1_	0x40000E12	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_2_	0x40000E14	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_3_	0x40000E16	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_4_	0x40000E18	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_5_	0x40000E1A	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_6_	0x40000E1C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_7_	0x40000E1E	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_8_	0x40000E20	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_9_	0x40000E22	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_10_	0x40000E24	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_11_	0x40000E26	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_12_	0x40000E28	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_13_	0x40000E2A	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_14_	0x40000E2C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_15_	0x40000E2E	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_16_	0x40000E30	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_17_	0x40000E32	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_18_	0x40000E34	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_19_	0x40000E36	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_20_	0x40000E38	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_21_	0x40000E3A	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_22_	0x40000E3C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_23_	0x40000E3E	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_24_	0x40000E40	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_25_	0x40000E42	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_26_	0x40000E44	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_27_	0x40000E46	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_28_	0x40000E48	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_29_	0x40000E4A	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_30_	0x40000E4C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_31_	0x40000E4E	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_32_	0x40000E50	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_33_	0x40000E52	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_34_	0x40000E54	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_35_	0x40000E56	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_36_	0x40000E58	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_37_	0x40000E5A	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_38_	0x40000E5C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_39_	0x40000E5E	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_40_	0x40000E60	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_41_	0x40000E62	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_42_	0x40000E64	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_43_	0x40000E66	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_44_	0x40000E68	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_45_	0x40000E6A	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_46_	0x40000E6C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_47_	0x40000E6E	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_48_	0x40000E70	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_49_	0x40000E72	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_50_	0x40000E74	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_51_	0x40000E76	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_52_	0x40000E78	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_53_	0x40000E7A	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_54_	0x40000E7C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_55_	0x40000E7E	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_56_	0x40000E80	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_57_	0x40000E82	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_58_	0x40000E84	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_59_	0x40000E86	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_60_	0x40000E88	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_61_	0x40000E8A	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_62_	0x40000E8C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_63_	0x40000E8E	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_64_	0x40000E90	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_65_	0x40000E92	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_66_	0x40000E94	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_67_	0x40000E96	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_68_	0x40000E98	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_69_	0x40000E9A	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_70_	0x40000E9C	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_71_	0x40000E9E	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_72_	0x40000EA0	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_73_	0x40000EA2	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_74_	0x40000EA4	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_75_	0x40000EA6	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_76_	0x40000EA8	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_77_	0x40000EAA	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_78_	0x40000EAC	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_79_	0x40000EAE	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_80_	0x40000EB0	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_81_	0x40000EB2	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_82_	0x40000EB4	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_83_	0x40000EB6	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_84_	0x40000EB8	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_85_	0x40000EBA	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_86_	0x40000EBC	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_87_	0x40000EBE	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_88_	0x40000EC0	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_89_	0x40000EC2	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_90_	0x40000EC4	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_91_	0x40000EC6	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_92_	0x40000EC8	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_93_	0x40000ECA	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_94_	0x40000ECC	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_95_	0x40000ECE	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_96_	0x40000ED0	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_97_	0x40000ED2	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_98_	0x40000ED4	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_99_	0x40000ED6	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_100_	0x40000ED8	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_101_	0x40000EDA	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_102_	0x40000EDC	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_103_	0x40000EDE	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_104_	0x40000EE0	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_105_	0x40000EE2	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_106_	0x40000EE4	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_107_	0x40000EE6	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_108_	0x40000EE8	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_109_	0x40000EEA	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_110_	0x40000EEC	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_111_	0x40000EEE	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_112_	0x40000EF0	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_113_	0x40000EF2	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_114_	0x40000EF4	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_115_	0x40000EF6	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_116_	0x40000EF8	0x0002	0x0000	RW	Bracketing look up table

Name	Address	Size	Reset Value	Access Type	Description
api_rw_bracketing_lut_117_	0x40000EFA	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_118_	0x40000EFC	0x0002	0x0000	RW	Bracketing look up table
api_rw_bracketing_lut_119_	0x40000EFE	0x0002	0x0000	RW	Bracketing look up table
api_rw_general_setup_ext_debug_out	0x40000FE0	0x0002	0x0000	RW/C	Debug parameter: Select output image source in ISP chain. 0 = Normal. See FW Guide or Application Notes for list of possible output points.
api_rw_general_setup_ext_otp_address_bpc	0x40000FEA	0x0002	0x0C40	RW	Address of Static BPC table in OTP.
api_ro_integration_time_capability	0x40001000	0x0002	0x0001	RO	0 = coarse integration but no fine integration. 1 = course and smooth (1 pixel) fine integration.
api_ro_integration_time_coarse_integration_time_min	0x40001004	0x0002	0x0002	RO	Minimum coarse integration in timing lines
api_ro_integration_time_coarse_integration_time_max_margin	0x40001006	0x0002	0x0002	RO	Current frame length - current max coarse exp
api_ro_integration_time_fine_integration_time_min	0x40001008	0x0002	0x0000	RO	Minimum fine integration in pixels
api_ro_integration_time_fine_integration_time_max_margin	0x4000100A	0x0002	0x0000	RO	Current line length - current max fine exp.
api_ro_digital_gain_capability	0x40001080	0x0002	0x0002	RO	0 = None. 1 = Per channel digital gain. 2 = Per channel or exposure digital gain (based on vendor_sensor_digital_gain_mode)
api_ro_digital_gain_min	0x40001084	0x0002	0x0100	RO	Minimum recommended digital gain value
api_ro_digital_gain_max	0x40001086	0x0002	0x8000	RO	Maximum recommended digital gain value

Name	Address	Size	Reset Value	Access Type	Description
api_ro_digital_gain_step_size	0x40001088	0x0002	0x0100	RO	Defines the resolution of the digital gain control parameters.
api_ro_pll_clock_limits_clock_tree_pll_capability	0x400010F0	0x0001	0x03	RO	Bit 0: 0 = 2-PLL clock tree not supported, 1 = 2-PLL clock tree supported. Bit 1: 0 = 1-PLL clock tree not supported, 1 = 1-PLL clock tree supported.
api_ro_pll_clock_limits_min_ext_clk_freq_mhz	0x400010F4	0x0004	0x41400000	RO	Minimum external clock frequency (IEEE754 format)
api_ro_pll_clock_limits_max_ext_clk_freq_mhz	0x400010F8	0x0004	0x42800000	RO	Maximum external clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_min_vt_pre_pll_clk_div	0x400010FC	0x0002	0x0001	RO	Minimum Pre PLL divider value
api_ro_pll_clock_limits_main_max_vt_pre_pll_clk_div	0x400010FE	0x0002	0x003F	RO	Maximum Pre PLL divider value
api_ro_pll_clock_limits_main_min_vt_pll_ip_freq_mhz	0x40001100	0x0004	0x40C00000	RO	Minimum PLL input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_pll_ip_freq_mhz	0x40001104	0x0004	0x41400000	RO	Maximum PLL input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_min_vt_pll_multiplier	0x40001108	0x0002	0x0040	RO	Minimum PLL multiplier
api_ro_pll_clock_limits_main_max_vt_pll_multiplier	0x4000110A	0x0002	0x03FF	RO	Maximum PLL multiplier
api_ro_pll_clock_limits_main_min_vt_pll_vco_freq_mhz	0x4000110C	0x0004	0x42200000	RO	Minimum VT PLL VCO frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_pll_vco_freq_mhz	0x40001110	0x0004	0x44960000	RO	Maximum VT PLL VCO frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_pll_post_scaler	0x40001114	0x0002	0x0004	RO	Maximum Post scaler S (2^S divider) value .
api_ro_pll_clock_limits_main_min_op_pll_freq_mhz	0x40001118	0x0004	0x42200000	RO	Minimum PLL output clock frequency (IEEE754 format)

Name	Address	Size	Reset Value	Access Type	Description
api_ro_pll_clock_limits_main_max_op_pll_freq_mhz	0x40001 11C	0x0004	0x44960000	RO	Maximum PLL output clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_min_vt_sys_clk_div	0x40001120	0x0002	0x0001	RO	Minimum video timing system clock divider value
api_ro_pll_clock_limits_main_max_vt_sys_clk_div	0x40001122	0x0002	0x000C	RO	Maximum video timing system clock divider value
api_ro_pll_clock_limits_main_min_vt_sys_clk_freq_mhz	0x40001124	0x0004	0x42200000	RO	Minimum video timing system clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_sys_clk_freq_mhz	0x40001128	0x0004	0x44960000	RO	Maximum video timing system clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_min_vt_pix_clk_div	0x4000112C	0x0002	0x0001	RO	Minimum video timing pixel clock divider value
api_ro_pll_clock_limits_main_max_vt_pix_clk_div	0x4000112E	0x0002	0x000C	RO	Maximum video timing pixel clock divider value
api_ro_pll_clock_limits_main_min_vt_pix_clk_freq_mhz	0x40001130	0x0004	0x42D80000	RO	Minimum video timing pixel clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_pix_clk_freq_mhz	0x40001134	0x0004	0x44160000	RO	Maximum video timing pixel clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_min_op_pre_pll_clk_div	0x40001138	0x0002	0x0001	RO	Minimum Pre OP PLL clock Divider Value
api_ro_pll_clock_limits_output_max_op_pre_pll_clk_div	0x4000113A	0x0002	0x003F	RO	Maximum Pre OP PLL clock Divider Value
api_ro_pll_clock_limits_output_min_op_pll_ip_freq_mhz	0x4000113C	0x0004	0x40C00000	RO	Minimum OP PLL input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_op_pll_ip_freq_mhz	0x40001140	0x0004	0x41400000	RO	Maximum OP PLL input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_min_op_pll_multiplier	0x40001144	0x0002	0x0010	RO	Minimum OP PLL Multiplier
api_ro_pll_clock_limits_output_max_op_pll_multiplier	0x40001146	0x0002	0x01FF	RO	Maximum OP PLL Multiplier
api_ro_pll_clock_limits_output_min_op_pll_vco_freq_mhz	0x40001148	0x0004	0x44160000	RO	Minimum OP PLL VCO frequency (IEEE754 format)

Name	Address	Size	Reset Value	Access Type	Description
api_ro_pll_clock_limits_output_max_op_pll_vco_freq_mhz	0x4000114C	0x0004	0x449C4000	RO	Maximum OP PLL VCO frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_op_pll_post_scaler	0x40001150	0x0002	0x0004	RO	Maximum Post scaler S (2^S divider) value .
api_ro_pll_clock_limits_output_min_op_pll_op_freq_mhz	0x40001154	0x0004	0x42160000	RO	Minimum OP PLL output clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_op_pll_op_freq_mhz	0x40001158	0x0004	0x449C4000	RO	Maximum OP PLL output clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_min_op_sys_clk_div	0x4000115C	0x0002	0x0001	RO	Minimum output system clock divider value
api_ro_pll_clock_limits_output_max_op_sys_clk_div	0x4000115E	0x0002	0x000C	RO	Maximum output system clock divider value
api_ro_pll_clock_limits_output_min_op_sys_clk_freq_mhz	0x40001160	0x0004	0x42160000	RO	Minimum output system clock frequency
api_ro_pll_clock_limits_output_max_op_sys_clk_freq_mhz	0x40001164	0x0004	0x449C4000	RO	Maximum output system clock frequency
api_ro_pll_clock_limits_output_min_op_pix_clk_div	0x40001168	0x0002	0x0001	RO	Minimum output pixel clock divider value
api_ro_pll_clock_limits_output_max_op_pix_clk_div	0x4000116A	0x0002	0x000C	RO	Maximum output pixel clock divider value
api_ro_pll_clock_limits_output_min_op_pix_clk_freq_mhz	0x4000116C	0x0004	0x41000000	RO	Minimum output pixel clock frequency
api_ro_pll_clock_limits_output_max_op_pix_clk_freq_mhz	0x40001170	0x0004	0x43300000	RO	Maximum output pixel clock frequency
api_ro_pll_clock_limits_output_min_dphy_freq_mhz	0x40001174	0x0004	0x42A00000	RO	Minimum DPHY input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_dphy_freq_mhz	0x40001178	0x0004	0x450660000	RO	Maximum DPHY input clock frequency (IEEE754 format)
api_ro_frame_timing_min_frame_length_lines	0x400011A0	0x0002	0x0064	RO	Minimum Frame Length allowed.
api_ro_frame_timing_max_frame_length_lines	0x400011A2	0x0002	0xFFFF	RO	Maximum possible number of lines per Frame.

Name	Address	Size	Reset Value	Access Type	Description
api_ro_frame_timing_min_line_length_pck	0x400011A4	0x0002	0x0000	RO	Minimum Line Length allowed. (0 = Auto select)
api_ro_frame_timing_max_line_length_pck	0x400011A6	0x0002	0xFFFF	RO	Maximum possible number of pixel clocks per line.
api_ro_frame_timing_min_line_blanking_pck	0x400011A8	0x0002	0x00B4	RO	Minimum line blanking time in pixel clocks
api_ro_frame_timing_min_frame_blanking_lines	0x400011AA	0x0002	0x0036	RO	Minimum frame blanking in video timing lines.
api_ro_frame_timing_min_line_length_pck_step_size	0x400011AC	0x0001	0x08	RO	Minimum step size of line length in pixel clocks
api_ro_size_limits_x_addr_min	0x400011B0	0x0002	0x0000	RO	Minimum X-address of the addressable pixel array
api_ro_size_limits_y_addr_min	0x400011B2	0x0002	0x0000	RO	Minimum Y-address of the addressable pixel array
api_ro_size_limits_x_addr_max	0x400011B4	0x0002	0x2000	RO	Maximum X-address of the addressable pixel array
api_ro_size_limits_y_addr_max	0x400011B6	0x0002	0x1820	RO	Maximum Y-address of the addressable pixel array
api_ro_size_limits_min_x_output_size	0x400011B8	0x0002	0x0100	RO	Minimum x output size in pixels
api_ro_size_limits_min_y_output_size	0x400011BA	0x0002	0x0090	RO	Minimum y output size in pixels
api_ro_size_limits_max_x_output_size	0x400011BC	0x0002	0x2000	RO	Maximum x output size in pixels
api_ro_size_limits_max_y_output_size	0x400011BE	0x0002	0x1820	RO	Maximum y output size in pixels
api_ro_sub_sample_min_even_inc	0x400011C0	0x0002	0x0001	RO	Minimum Increment for even pixels
api_ro_sub_sample_max_even_inc	0x400011C2	0x0002	0x0002	RO	Maximum increment for even pixels
api_ro_sub_sample_min_odd_inc	0x400011C4	0x0002	0x0001	RO	Minimum Increment for odd pixels

Name	Address	Size	Reset Value	Access Type	Description
api_ro_sub_sample_max_odd_inc	0x400011C6	0x0002	0x000F	RO	Maximum Increment for odd pixels
api_ro_scaling_scaling_capability	0x40001200	0x0002	0x0002	RO	0 = None. 1 = Horizontal. 2 = Full (Horizontal & Vertical)
api_ro_scaling_scaler_m_min	0x40001204	0x0002	0x0010	RO	Down scale factor: Minimum M value (x1 - No scale)
api_ro_scaling_scaler_m_max	0x40001206	0x0002	0x0080	RO	Down scale factor: Maximum M value (x4 scale)
api_ro_scaling_scaler_n_min	0x40001208	0x0002	0x0010		
api_ro_scaling_scaler_n_max	0x4000120A	0x0002	0x0010		
api_ro_scaling_spatial_sampling_capability	0x4000120C	0x0002	0x0001		
api_ro_scaling_digital_crop_capability	0x4000120E	0x0002	0x0001	RO	0 = None. 1 = input digital crop supported.
api_ro_compression_capability	0x40001300	0x0002	0x0001	RO	Image Compression Capability Register - [0x1300-0x1301] 0 = None. 1 = DPCM/PCM.
api_ro_fifo_size_pixels	0x40001500	0x0002	0x0000		
api_ro_fifo_support_capability	0x40001502	0x0001	0x02	RO	0 = not supported. 1 = supports derating. 2 = supports VT/OP domain decoupling.
api_ro_dphy_ctrl_capability	0x40001600	0x0001	0x1F	RO	Bit 0: 1 = automatic DPHY control supported.

Name	Address	Size	Reset Value	Access Type	Description
					Bit 1: 1 = UI based DPHY control supported. Bit 2: 1 = manual register control based DPHY control supported for non-extended Time_and_UI_1 register. Bit 3: 1 = manual register control based DPHY control supported for non-extended Time_and_UI_2 register. Bit 4: 1 = manual register control based DPHY control supported for non-extended Time register.
api_ro_dphy_lane_mode_capability	0x40001601	0x0001	0x0F	RO	Bit 0: 1 = 1 lane supported, 0 = not supported. Bit 1: 1 = 2 lane supported, 0 = not supported. Bit 2: 1 = 3 lane supported, 0 = not supported. Bit 3: 1 = 4 lane supported, 0 = not supported.

Name	Address	Size	Reset Value	Access Type	Description
					Bit 4: 1 = 5 lane supported, 0 = not supported. Bit 5: 1 = 6 lane supported, 0 = not supported. Bit 6: 1 = 7 lane supported, 0 = not supported. Bit 7: 1 = 8 lane supported, 0 = not supported.
api_ro_dphy_signalling_mode_capability	0x40001602	0x0001	0x04	RO	Bit 0: PVI. Bit 1: reserved. 2 = CSI-2 with D-PHY supported. 0 = not supported.
api_ro_dphy_fast_standby_capability	0x40001603	0x0001	0x01	RO	0 = Frame truncation not supported for rolling shutter. 1 = Frame truncation supported for rolling shutter.
api_ro_dphy_cci_address_control_capability	0x40001604	0x0001	0x00	RO	Bit 0: 1 = SW changeable CCI address supported. 0 = not supported.
api_ro_binning_min_frame_length_lines_bin	0x40001700	0x0002	0x0064	RO	Minimum frame length in timing lines on binning mode.
api_ro_binning_max_frame_length_li	0x4000	0x0	0xFFF		Maximum frame length in timing lines

Name	Address	Size	Reset Value	Access Type	Description
nes_bin	1702	002	F	RO	on binning mode.
api_ro_binning_min_line_length_pck_bin	0x40001704	0x0002	0x0000	RO	0 = FW choose shortest length lines possible. Otherwise, this is the minimum value.
api_ro_binning_max_line_length_pck_bin	0x40001706	0x0002	0xFFFF	RO	Maximum frame length in timing lines on binning mode.
api_ro_binning_min_line_blanking_pck_bin	0x40001708	0x0002	0x00B4	RO	Minimum line blank time in Pixel clocks.
api_ro_binning_fine_integration_time_min_bin	0x4000170A	0x0002	0x0000	RO	Minimum fine integration time allowed in binning mode.
api_ro_binning_fine_integration_time_max_mar_bin	0x4000170C	0x0002	0x0000	RO	Margin used to determine the maximum fine integration time allowed in binning mode.
api_ro_binning_binning_capability	0x40001710	0x0001	0x01	RO	Bit 0: 0 = No. 1 = Yes.
api_ro_binning_binning_weighting_capability	0x40001711	0x0001	0x01	RO	Bit 0: 1 = Averaged Bit 1: 1 = Summed (for low light) Bit 2: 1 = Bayer-corrected Bit 3: 1 = Module specific weighting.
api_ro_binning_binning_sub_types	0x40001712	0x0001	0x05	RO	Number of Binning subtypes available.
api_ro_binning_binning_type_1	0x4000	0x0	0x11		Supported analog binning

Name	Address	Size	Reset Value	Access Type	Description
	1713	001		RO	Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_2	0x40001714	0x0001	0x12	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_3	0x40001715	0x0001	0x13	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_4	0x40001716	0x0001	0x14	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_5	0x40001717	0x0001	0x16	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_6	0x4000	0x0	0x11		Supported analog binning

Name	Address	Size	Reset Value	Access Type	Description
	1718	001		RO	Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_7	0x40001719	0x0001	0x11	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_8	0x4000171A	0x0001	0x11	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_9	0x4000171B	0x0001	0x11	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_10	0x4000171C	0x0001	0x11	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_11	0x4000	0x0	0x11		Supported analog binning

Name	Address	Size	Reset Value	Access Type	Description
	171D	001		RO	Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_12	0x4000 171E	0x0 001	0x11	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_binning_binning_type_13	0x4000 171F	0x0 001	0x11	RO	Supported analog binning Bits[7:4] = columns binning factor. Bits[3:0] = rows binning factor.
api_ro_data_transfer_if_capability	0x4000 1800	0x0 001	0x01	RO	Bit 0: 1 = interface 1 supported Bit 1: reserved, report value 0. Bit 2: 0 = polling not needed in reading. 1 = polling needed in reading. Bit 3: 0 = polling not needed in writing.

Name	Address	Size	Reset Value	Access Type	Description
					1 = polling needed in writing. Bit 4: 0 = supports single DTI functionality. 1- supports multi DTI functionality Bits 0-3 are valid in single DTI functionality only
api_ro_isp_shading_correction_capability	0x40001900	0x0001	0x03	RO	Bit 0: 1 = On-module shading correction. Bit 1: 1 = Luminance correction adjust available.
api_ro_isp_green_imbalance_capability	0x40001901	0x0001	0x00	RO	Bit 0: 1 = on-module green imbalance filtering. Bit 1: 1 = Green imbalance filter weight adjust available.
api_ro_isp_black_level_capability	0x40001902	0x0001	0x01	RO	Bit 0: 1= On module black level correction.
api_ro_isp_module_specific_correction_capability	0x40001903	0x0001	0x00		Bit 0: 0 = not supported. 1 = Manuals supported. Bit 1: 0 = not supported.

Name	Address	Size	Reset Value	Access Type	Description
					1 = Limited auto supported.
api_ro_isp_defect_correction_capability	0x40001904	0x0002	0x40FD	RO	Bit 0: 1= internal module mapped defect correction available. Bit 1: 1= internal module mapped defect correction weight available. Bit 2: 1= internal module dynamic couplet correction available. Bit 3: 1= manual dynamic couplet correction weight adjust available. Bit 4: 1= limited auto dynamic couplet correction weight adjust available. Bit 5: 1= internal module dynamic single pixel defect correction available. Bit 6: 1= manual dynamic single pixel defect correction weight adjust available.

Name	Address	Size	Reset Value	Access Type	Description
					Bit 7: 1= limited auto dynamic single pixel defect correction weight adjust available. Bit 8: 1= combined internal module dynamic couplet & single pixel defect correction available. Bit 9: 1= manual dynamic couplet & single pixel defect correction weight adjust available. Bit 10: 1 = limited auto dynamic couplet & single pixel defect correction weight adjust available. Bits 11-B13: reserved Bit 14: 1= mapped defect limited auto weight adjust available Bit 15: reserved for future extensions
api_ro_isp_defect_correction_capabi	0x4000	0x0	0x0000		Bit 0:

Name	Address	Size	Reset Value	Access Type	Description
lity_2	1906	002		RO	1 = internal module mapped triplet correction available. Bit 1: 1 = manual mapped triplet correction weight adjust available. Bit 2: 1 = limited auto mapped triplet correction weight adjust available. Bit 3: 1 = internal module dynamic triplet correction available. Bit 4: 1 = manual dynamic triplet correction weight adjust available. Bit 5: 1 = limited auto dynamic triplet correction weight adjust available. Bit 6: 1 = internal module dynamic line correction available. Bit 7:

Name	Address	Size	Reset Value	Access Type	Description
					1 = manual dynamic line correction weight ajust available. Bit 8: 1 = limited auto dynamic line correction weight adjust available. Other bits: reserved for future extensions.
api_ro_color_feedback_capability	0x4000 19B0	0x0 001	0x02	RO	Bit 0 : Module requires Kelvin feedback. Bit 1 : Module requires AWB Gain feedback.
api_ro_static_af_camera_actuator_type	0x4000 1B40	0x0 002	0x0000	RO	Reserved for host usage for the mentioned purpose.
api_ro_static_af_camera_af_device_address	0x4000 1B42	0x0 001	0x00	RO	I2C address of AF device.
api_ro_pdaf_capability	0x4000 1B80	0x0 001	0xF5	RO	Bit 0: 1 = PDAF supported. Bit 1: 1 = processed PDAF data readout in bottom embedded data. Bit 2: 1 = processed PDAF data readout in interleaved manner.

Name	Address	Size	Reset Value	Access Type	Description
					Bit 3: 1 = RAW PDAF data readout in bottom embedded data. Bit 4: 1 = RAW PDAF data readout in interleaved manner. Bit 5: 1 = visible pixel area PDAF pixel specific defect correction supported. Bit 6: 1 = virtual channel interleaving supported. Bit 7: 1 = data type interleaving supported.
api_ro_bracketing_lut_capability_1	0x40001C00	0x0002	0x0033	RO	Bit 0: 1 = coarse integration time LUT entry supported Bit 1: 1 = global analog gain LUT entry supported Bit 2. reserved. Bit 3: reserved. Bit 4:

Name	Address	Size	Reset Value	Access Type	Description
					1 = flash LUT entry supported. Bit 5: 1 = global digital gain LUT entry supported. Bit 6-7: reserved for future use. All bits: 0 = not supported
api_ro_bracketing_lut_capability_2	0x40001C02	0x0001	0x03	RO	Bit 0: 1 = supports single bracketing mode. Bit 1: 1 = supports looped bracketing mode.
api_ro_bracketing_lut_size	0x40001C03	0x0001	0x1E	RO	Max number of frames supported by LUT, e.g. 5 = LUT can contain settings for 5 frames. 240 bytes, 4 field types, each field type is 2 bytes,